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# Theoretical Modeling of Single-Phase Power Electronics Loads to Predict Harmonic Distortion at a Distribution Feeder Network using a Reverse Optimization Solution

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# Theoretical Modeling of Single-Phase Power Electronics Loads to Predict Harmonic Distortion at a Distribution Feeder Network using a Reverse Optimization Solution

**by**

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To family and friends

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# Theoretical Modeling of Single-phase Power Electronics Loads to Predict Harmonic Distortion at a Distribution Feeder Network using a Reverse Optimization Solution

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Supervisor: W. Mack Grady

Proliferation of non-linear, single-phase power electronics loads, such as personal computers, television sets, CFLs, has resulted in thousands of individual small harmonic current injectors connected to a distribution feeder network. Harmonic standard: *IEC 1000-3-2* classifies such loads as Class D, "low-voltage" equipment with current emissions limited to 16A/Phase. Individual harmonic contributions of such loads appear insignificant; their collective contribution, however, is a matter of concern. The average order of voltage distortion usually varies between 4-6%; current distortion, however, is usually of the order of 100%. Limitations and high-costs associated with conventional harmonic mitigation measures, has furthered the need for regulation and alternative strategies.

The objective of this research is to predict, and mitigate the effects of harmonic proliferation in the main supply current measured at the point of common coupling (PCC). An equivalent circuit model – an aggregation of single-phase power electronics loads connected to the distribution feeder network is proposed as a part of a *forward* solution. Each load, individually, behaves as a harmonic current source; the proposed model combines these individual harmonic current injectors into a single harmonic source connected at the PCC and their collective contribution as a single composite harmonic signal. It represents harmonic conditions at the PCC and provides a theoretical measure of harmonic distortion in the supply current.

Such a model finds application during harmonic compliance testing for single-phase power electronics loads; it simulates and predicts the harmonic response of such loads using a theoretical pure 60 Hz sine wave as the supply voltage diffcult to obtain physically, yet critical to such tests.

The accuracy of the equivalent circuit model in predicting a harmonic response is pivotal to a successful *forward* solution. A *feed-backwards* mechanism is proposed. For a given harmonic supply voltage and circuit configuration of the equivalent circuit model, the *feed-backwards* method generates the modeled response and compares it to a reference physical response. Finally, it optimizes the circuit configuration to a unique *Correction Factor* that facilitates an accurate modeled response. Three optimization algorithms, labeled as *Response Optimization algorithms* have been developed to execute the *feed-backwards* mechanism. These algorithms are written in FORTRAN-90.

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# CHAPTER 1

# Introduction

## 1. SYNOPSIS

To conduct successful harmonic analysis at a distribution-feeder network, the source of harmonic distortion must be identified. Historically, such harmonic sources were attributed to one or few large power-electronics loads connected at the point of common coupling (PCC), an adjustable speed-drive, for instance. However, in little over a decade, progressive proliferation of single-phase power-electronics loads, such as personal computers, has resulted in thousands of individual small harmonic current injectors connected to a common distribution-feeder network. Though their individual contributions might be insignificant, such proliferation causes significant harmonic distortion that cannot be ignored.

Thus, in order to perform harmonic mitigation analysis at a distribution-feeder network, collective harmonic impact of all single-phase power electronics loads connected to the network must be considered.

A *forward* solution is proposed to proactively predict, and mitigate the effects of harmonic proliferation as they impact the supply current, these effects are due to the large number of single-phase power electronics loads connected to the distribution feeder network. An equivalent circuit model – an aggregation of all single-phase power electronics loads connected at the point of common coupling is proposed as part of the *forward* solution. If we liken each single-phase power electronics load to a fixed harmonic current injector; we can derive a model that simulates all harmonic current-

injectors, collectively, as a single source, thus combining their individual contributions as a single composite harmonic signal. The model simulates the harmonic conditions at the point of common coupling, which allows us to predict the harmonic supply current flowing through it. The proposed model represents a single power electronics load as well as a collection of such loads connected to the same network and it then predicts their response. Evidently, then, we should start by creating a model for a single load, and then extend it to multiple loads connected to a given network.

The equivalent circuit model is designed with the point of common coupling (PCC) as its point of reference. where the distribution-feeder is connected to a composite single-phase power electronics load via a diode-bridge rectifier circuit.

The distribution feeder is modeled as a Thevenin's equivalent of a harmonic voltage source connected to the PCC via Thevenin's equivalent impedance, and shared-transformer impedance. Elements of the Diode Bridge Rectifier circuit include, Discharging Capacitance $C$, system impedance, expressed collectively as $R_{TRAN}$ and $L_{TRAN}$, internal impedance of the rectifier circuit $R_1$ and $L_1$ and the load resistance $R_L$.

The rectifier circuit converts input AC voltage, observed at the PCC, to a rectified DC output. This DC output voltage is input to the composite power electronics load. The process of AC – DC rectification of the supply-voltage generates a periodic input current pulse, $I_S$, that charges the smoothing-capacitor of the diode bridge rectifier circuit. This charging current, high in harmonic content, is ultimately injected back into the main current supply, thus, increasing harmonic content of the supply.

The response of the equivalent circuit model, as stated earlier, is measured in terms of the input harmonic current pulse $I_S$. To successfully create such a model; it is imperative to ensure the accuracy of its response. This requires comparing the response

of the equivalent circuit to a reference physical response, and correcting it by optimizing its circuit parameters such that it emulates the physical response accurately. This method of correcting the response of the equivalent circuit model and determining an optimized circuit configuration is called the *feed-backwards* solution.

The *feed-backwards* solution is at the core of this research. It involves comparing and correcting the simulated response of the circuit model, expressed in terms of the charging input current pulse $I_{S,MOD}$ to the actual physical response, $I_{S,MEAS}$. For a particular combination of the circuit parameters, which we label collectively as the *Correction Factor*, if the simulated response replicates the physical response of the system, within a measure of accuracy, the equivalent-circuit model is said to be valid. It, therefore, accurately predicts the harmonic response generated at a distribution-feeder network with thousands of single-phase power electronic harmonics-injecting sources connected to it.

Three optimization algorithms, called the *Response Optimization Algorithms*, are proposed as a part of the *feed-backwards solution*. The *Load Response* algorithm generates the simulated response, $I_{S,MOD}$, of the equivalent-circuit model, for a 120 $V_{RMS}$ harmonic supply-voltage input and a set of circuit parameters values; the *Error Calculation* algorithm determines the difference between $I_{S,MOD}$ and the physical response, $I_{S,MEAS}$. Finally, the *Error Optimization* algorithm optimizes the circuit parameters to correct the modeled response and match it to its reference physical response. *Error Optimization* is an iterative process that employs the *Load Response* and the *Error Calculation* algorithms to generate the simulated response and calculate its difference from the reference physical value for every optimization iteration.

Hence, a successful *forward* solution requires an accurate equivalent circuit model. The accuracy of the modeled response is corrected, verified, and validated using a *feed-backwards* optimization solution. This research delves into the development of such a solution.

The harmonic standards mandate the compliance of the single-phase power electronics loads to the prescribed regulations. However, one measure of such compliance based on the assumption that a pure sinusoidal supply voltage be used for testing purposes is difficult to achieve in practical terms. In order to adhere to harmonic standards, we need to energize power electronics loads with standard AC voltage, THDV ~ 2 - 5%, from a regular wall outlet, for instance; perform tests; and correct the testing results in such a way that the harmonics content of the resultant load current matches that of a load current produced in a perfect sinusoidal input voltage scenario.

Development of the proposed *forward* solution will enable us to perform compliance tests using as a reference a current pulse $I_{S,MEAS}$, generated for a pure theoretical 60 Hz sine-wave as the supply voltage. This will enable us the ability to correct the modeled response, $I_{S,MOD}$, against the theoretical reference using the *feed-backwards* approach, ensuring that the current response of the given single-phase power electronics load or the collective supply current at the PCC does not exceed the prescribed harmonic limits.

A *Harmonics Testing Station* – an experimental equivalent of the proposed analytical model is used to verify the simulated theoretical response of the proposed equivalent-circuit model and can therefore validate and determine whether the *forward* and the *feed-backwards* solutions generate the appropriate response.

A LabView based experimental set-upthe *Harmonics Testing Station* is designed to examine the voltage conditions and conduct harmonic mitigation analysis at the point

of common coupling (PCC). It executes a correction mechanism to alleviate the harmonic content of the voltage at PCC. I was one of several students who developed the testing-station under supervision of Dr. Grady over several years

An experiment, with a composite load connected to a harmonic voltage source is simulated by connecting that load to the *Harmonics Testing Station*. The results of that experiment have been used to illustrate the accuracy of the equivalent circuit model in terms of its response via the harmonic input current pulse $I_S$.

## 2. BACKGROUND AND PAST EFFORTS

*Background*

Most of today's information technology equipment, appliances and lighting equipment fall under the classification of non-linear loads; they utilize motor controls, power supplies, and ballasts to improve cost, size, weight and/or efficiency. However, design imperfections may cause these devices to draw a load current of high harmonic content from power distribution systems. Widely distributed single-phase power electronic loads such as desktop computers, television sets, microwave ovens, fluorescent lights and compact fluorescent lights is one such class of equipment; it is an important source of harmonics in power distribution systems. Individually, these products are generally low power with the currents less than 16 A, but as these loads continue to proliferate, and larger non-linear loads (such as adjustable speed drives, heat pumps and electric battery chargers) are employed, the cumulative harmonics become significant and cannot be ignored. A number of these loads together can cause nuisance tripping of circuit breakers, fire hazards, and interference in the performance of other devices.

The impact of supply-voltage and current distortion on the performance of these devices merits further explanation. Most of these loads are designed to operate at pure 60 Hz sinusoidal input voltage. Harmonic proliferation in the supply-voltage, caused by single-phase power electronics loads connected to the power distribution system (also referred to as the Point of Common Coupling, PCC), adversely affects their function through reduced performance and efficiency, higher heating and operating losses and, reduced life span. Ironically, as more of these devices become a part of the network, they exacerbate harmonic distortion in the network that affects all devices, and the process of contamination continues unabated. A vicious cycle is thus established; proliferation of single-phase power electronics loads into the network, increases harmonic distortion, both at the device level and at the PCC, to magnitudes harmful to the very devices causing it. While the supply-voltage distortion is usually limited to the order of 5%,; current distortion manifests itself to the order of 100%, while it's accepted range is less than 10%.

Efforts are, therefore, underway to limit the harmonic currents produced by these loads. Traditional methods of harmonic line current reduction include, deployment of line-filters using passive components or active electronic circuitry. Two methods of harmonic reduction are proposed, *Passive Harmonic Current Reduction* and *Active Harmonic Line Current Reduction*.

*Pass Efforts*

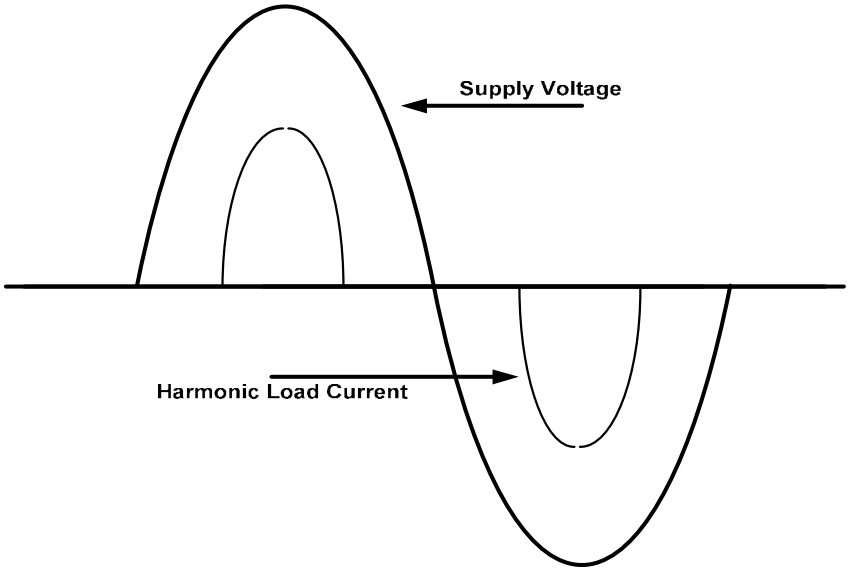



**Figure 1.1: Harmonic Current without Harmonic Reduction**

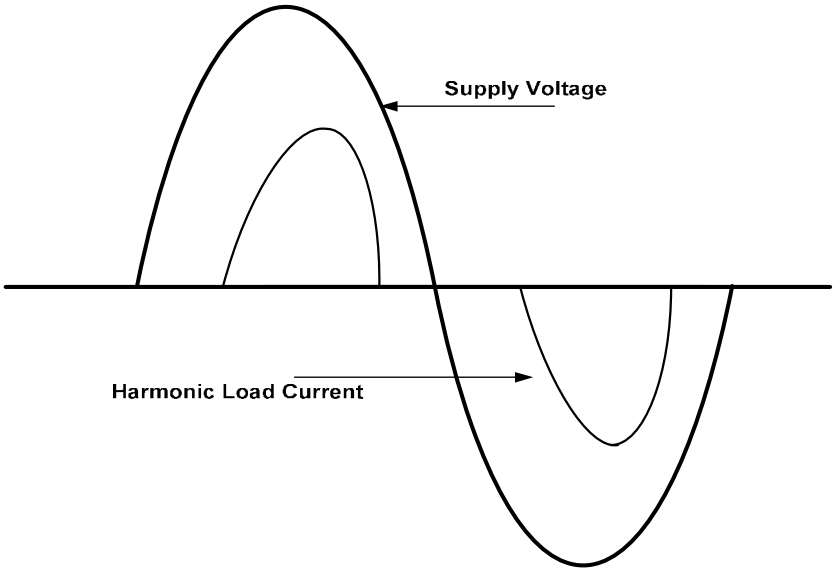



**Figure 1.2: Harmonic Current with Passive Harmonic Reduction**

- *Passive Harmonic current reduction:* Harmonic line current reduction using passive components (inductors and capacitors) introduces high impedance for the harmonics which smoothes out the harmonic load current.

  Passive harmonic current reduction usually involves a simple robust circuitry which is usually less expensive than active harmonic line reduction. There are two problems with this solution, however, It is dependent on large and heavy low-frequency magnetics and it is not applicable for wide input range and higher power. The non-sinusoidal shape of resultant harmonic current suggests residual harmonic content, as illustrated in Figure 1.2.
- *Active Harmonic Line Current Reduction:* Harmonic load current reduction using active electronic circuitry, shapes the input current of an electronic equipment in proportion to the applied line voltage, thus, rendering a sinusoidal input current, in phase with the line voltage as shown in Figure 1.3. The corresponding circuitry is often called the *Power Factor Correction (PFC)* circuitry.

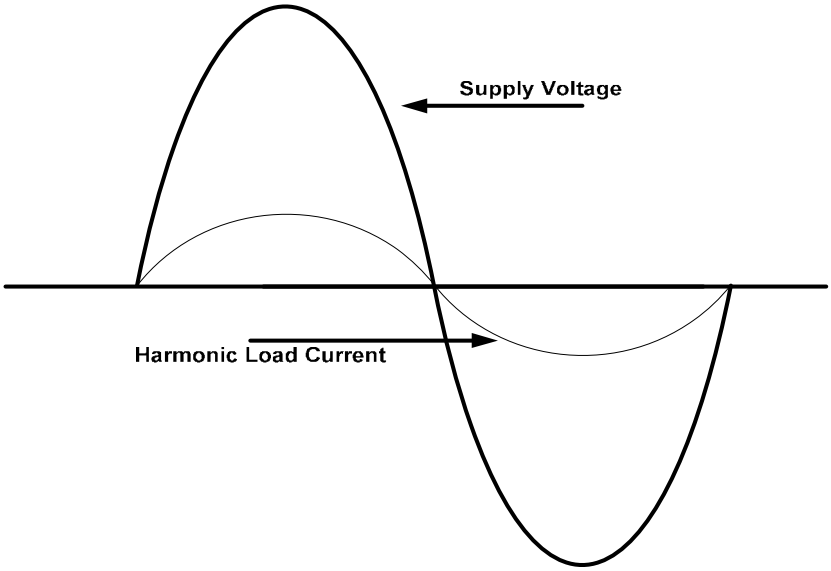



**Figure 1.3: Harmonic Current with Active Harmonic Reduction**

Active harmonic line current reduction is an effective means of harmonic mitigationthat causes extensive elimination of line current harmonics, with a resultant power factor close to 1 (with the uncorrected power factor being approximately 0.6). This increases power factor availability from a wall outlet. On the other hand, this approach is more expensive due to the circuitry involved and increased number of constituent parts, and it adversely affects the efficiency of the power electronics equipment being filtered.

Given the exponential rise in the deployment of single-phase power electronic devices over the past two decades, we need alternative strategies and methods to contain harmonic distortion. These strategies will aim at solving the problem of the traditional inaccessibility of the physical locations where these filters (active or passive) are installed, and at the same time lower the high costs involved in dealing with these distortions.

## 3. HARMONIC STANDARDS

Power electronics equipments such as Switched Mode Power Supplies (SMPS), a subset of the single-phase power electronics loads, can be designed to provide harmonic-free, unity power-factor performance. Advances in electronics, both power and control, have provided designers with new and more cost-effective options to clean up the interface with the power system. However, the economic incentives have not been sufficient to bring about significant design improvements in most applications.

The power system community worldwide, therefore, has turned to legislation and regulation to force the use of lower-harmonic electronic power supply designs. Their common objective is to preserve the sinusoidal nature of power system supply-voltage while protecting power system components from harmonic (mainly) current loading. This effort has translated into the development and implementation of harmonic standards. Amongst the various harmonic standards, *EN-61000-3-2 (or IEC 1000-3-2), IEC 1000-3-4 and IEEE 519* are the most cited standards in the regulation of harmonic distortion in single-phase power electronics loads. The *IEC 1000-3-2* sets limits on the harmonic current emissions for equipment input current less than or equal to 16 Amperes/phase. It sets limits for small customer's equipment with emphasis on "public", "low voltage" and "households". *IEC1000-3-4* deals with individual equipment and sets limits for the whole system installation addressing both single-phase and three-phase harmonic limits. The *IEEE-519-1992* standard sets limits on harmonic voltage and current at the point of common coupling (PCC). The philosophy behind this standard is to prevent harmonic currents bouncing back to the power system and affecting other customers. Table 1.1 summarizes the protection mandated by the IEC and IEEE harmonics.

| Harmonic Limiting Standards | | Small Consumer | | Large Consumer | | Utility Power System |
|---|---|---|---|---|---|---|
| | | Loads/Wiring | Service Entrance | Loads/Wiring | Service Entrance | |
| IEEE 519 (1992) | I | No | No | Yes | Yes | Yes |
| | V | No | Yes | Yes | Yes | Yes |
| IEC 1000-3-2 | I | Yes | Yes | No | No | No |
| | V | No | No | No | No | No |
| IEC 1000-3-4 | I | No | No | Yes | Yes | Yes |
| | V | No | No | No | No | No |

**Table 1.1: Summary of IEEE519 and IEC1000-3-2/4 Applicable Areas**

The harmonic standards mandate the compliance of the single-phase power electronics loads to the prescribed regulations. However, a measure of such compliance is based on the assumption that a pure sinusoidal supply voltage be used for testing purposes even though such voltage is difficult to achieve in practical terms. Thus, there exists a need to energize power electronics loads with standard AC voltage, THDV ~ 2 - 5%, from a regular wall outlet, for instance, perform tests, and correct the testing results in a way that the harmonics content of the resultant load current matches that of a load current produced in a perfect sinusoidal input voltage scenario.

Therefore, we have explored the ability of the *forward solution* to simulate the physical response of a single-phase power electronics load in order to facilitate successful harmonics testing. The physical response of the power electronics load, powered by a pure 60 Hz sinusoidal voltage is taken as our reference. The *Response Optimization algorithms,* as a part of the *feed-backwards* solution, correct the simulated response of the

load to match the reference response, which thus determines the optimized circuit parameter values of an equivalent circuit that would ensure an accurate simulation of a reference physical 60 Hz response.

In this way, the forward solution ensures that neither the current response of the given single-phase power electronics load, nor the collective supply current at the PCC exceeds the prescribed harmonic limits.

4. ***FEED-BACKWARDS* SOLUTION** – CREATING AN ACCURATE EQUIVALENT CIRCUIT MODEL

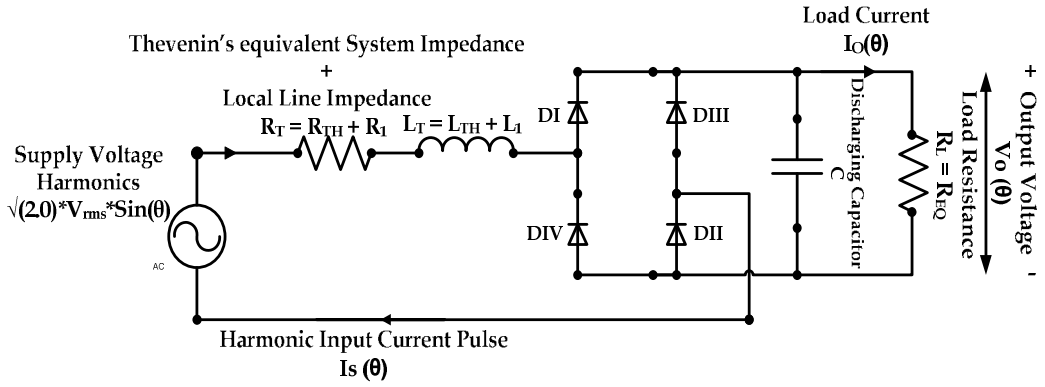



**Figure 1.4: Capacitor Filtered Diode-Bridge Rectifier Model**

The *feed-backwards* solution entails the development of an equivalent circuit model and the correction of its modeled response to accurately emulate a real physical response. The model so developed represents a distribution feeder network connected to a multitude of single-phase power electronics loads and powered by a harmonic voltage source.

In order to perform harmonic mitigation analysis at a distribution-feeder network, the collective harmonic impact of all single-phase power electronics loads connected to

the distribution-feeder must be considered. An equivalent-circuit model – an aggregation of all single-phase power electronics loads connected at the point of common coupling is proposed. In such a model, a harmonic voltage source is connected to a resistive load through a diode-bridge rectifier circuit in order to simulate all harmonic current-injectors collectively as a single source, and fold their combined individual contributions into a single composite harmonic signal. This approach constitutes the *forward* solution.

Circuit analysis of a single-phase power electronics load is performed; an analytical model for the given circuit is devised – it is expressed as the mathematical representation of the charging input current pulse, $I_S$ and the rectified output voltage $V_O$. The response of the circuit model, however, is measured only in terms of its input current pulse, $I_{S^1}$.

Each single-phase power electronics load entails a single-phase diode-bridge rectifier circuit that converts the input AC to a rectified DC voltage powering a single-phase power electronics load. Harmonic distortion in single-phase power electronics load is mostly attributable to the rectifier circuit. The process of AC – DC rectification of the supply-voltage generates a periodic input current pulse, $I_S$, that charges the smoothing-capacitor filter of the diode bridge rectifier circuit. This charging current, high in harmonic content (due to the presence of non-linear components of the rectifier circuit), is ultimately injected back into the main current supply which increases the harmonic content of the main current.

The voltage at the point-of-common couplingas well as the combined system and load impedances all affect harmonic current, $I_S$; system impedance, in turn, increases as

[1] The mathematical expression of current pulse can be broken down into its Fourier coefficients where each individual coefficient corresponds to an odd harmonic. Conversely, the sum (or superposition) of all these harmonics constitute the composite harmonic load current. Even-ordered harmonics are of a negligible magnitude and their presence usually indicates an anomaly in the current pulse.

the distance lengthens between the load and the point of common coupling. This means that for a fixed voltage at the point of common coupling, the greater the distance, the higher the system impedance and the smaller is the magnitude of the harmonic current.

The analytical model of the equivalent-circuit, as a part of the *forward* solution, enables us to predict and simulate its response to a given harmonic supply voltage. For a successful implementation of the model, however, the accuracy its response is vital. A *feed-backwards* method is proposed to serve this objective.

*The feed-backwards solution employs Response Optimization algorithms* to simulate the load response of the input current pulse, $I_S$ (which is the measure of the response of the circuit model. The algorithms also identify the difference between the modeled response and its physical equivalent, and correct the modeled load response so that it matches the physical response by optimizing the circuit parameters of the equivalent-circuit model.

## *5. RESPONSE OPTIMIZATION ALGORITHMS*

The analytical model of the equivalent-circuit is a mathematical expression of its input current pulse, $I_S$. The response of the equivalent-circuit and the (harmonic) quality of that response is measured in terms of the current $I_S$. Three algorithms, collectively labeled as *Response Optimization algorithms,* are written to implement the equivalent-circuit and model its response accurately to a simulate reference physical response.

The first amongst them is called the *Load Response* algorithm. It executes the analytical model and simulates the input current pulse, $I_S$, for a given input harmonic supply-voltage. This modeled current pulse is denoted as $I_{S,\ MOD}$ while the reference physical response is labeled as $I_{S,\ MEAS}$.

The difference between the simulated and the physical response of the system is determined using the second of our algorithms, called an *Error Calculation* algorithm. It is measures as the difference between the currents, $I_{S,MEAS}$ and $I_{S,MOD}$. This difference is determined either as the sum of differences between the values of two current pulses, calculated at each degree for a complete 360-degrees cycle, or as the difference between the harmonic (Fourier) coefficients of the two current pulses.

Finally, the third in our set is called the *Error Optimization* algorithm. It is implemented to optimize the circuit parameters $C$, $R_L$, $R_T$ and $L_T$ in order to make the simulated response $I_{S,MOD}$ closely match the physical response $I_{S,MEAS}$. The *Error Optimization* algorithm minimizes the simulated-to-physical response difference through an iterative feedback correction mechanism in which the circuit parameters $C$, $R_L$, $R_T$ and $L_T$ are sequentially varied. The parameter most sensitive to error minimization is varied during iteration while the rest are held constant. *Load Response* of the rectifier circuit is then determined with the revised parameters values, which permits the generation of the corrected simulated response $I_{S,MOD}$ for that iteration. The *Error Calculation* algorithm updates the difference between $I_{S,MOD}$ and the reference physical response $I_{S,MEAS}$. The process repeats with next most sensitive parameter varied; it continues until the simulated response is able to replicate the physical response, within a measure of accuracy, for a unique set of optimized circuit parameters labeled as the *Correction Factor*.

Having successfully performed *Error Optimization* and having determined a unique solution of parameters, we have now designed an equivalent-circuit model. We now possess the ability to theoretically predict the response $I_S$ of that physical system being modeled, for a supply-voltage input with any harmonic content (including a pure 60 Hz sinusoidal voltage). The three *Response Optimization algorithms – Load Response,*

*Error Calculation* and *Error Optimization,* have been written and executed in FORTRAN-90.

## 6. HARMONICS TESTING STATION

The *Harmonics Testing Station* is a LabView based experimental set-up, designed to examine the voltage conditions and conduct harmonic mitigation analysis at the point of common coupling (PCC). It executes a correction mechanism to alleviate the harmonic content of the voltage at PCC. I was one of the several students participating in the development of the testing-station over several years.

The testing station can be viewed as the experimental equivalent of the proposed analytical model of single-phase power electronics loads connected to the distribution-feeder network, and powered by a sinusoidal harmonic voltage source. It is used to verify the simulated theoretical response of the proposed equivalent-circuit and thus validate the analytical model, the *forward* and the *feed-backwards* solutions generating that response.

The analytical (equivalent circuit) model is considered valid under the following condition: the analytical model, powered by a supply-voltage with user-defined harmonic content, generates a theoretical response $I_S$, and a unique *Correction Factor* that is found to be consistent with the physical response, generated in an experimental set-up consisting of multiple (or one) single-phase power electronics loads connected to the Testing Station.

An experiment, with a composite load connected to a harmonic voltage source, is simulated by connecting that load to the *Harmonics Testing Station*. The results of that experiment have been used to illustrate the accuracy of the equivalent circuit model in terms of its response – the input current pulse $I_S$. These results also demonstrate the utility

of the *Harmonics Testing Station* as a tool to benchmark the response of the proposed equivalent circuit model.

# CHAPTER 2

## Introduction to Single-phase Power Electronics Loads

### 1. INTRODUCTION

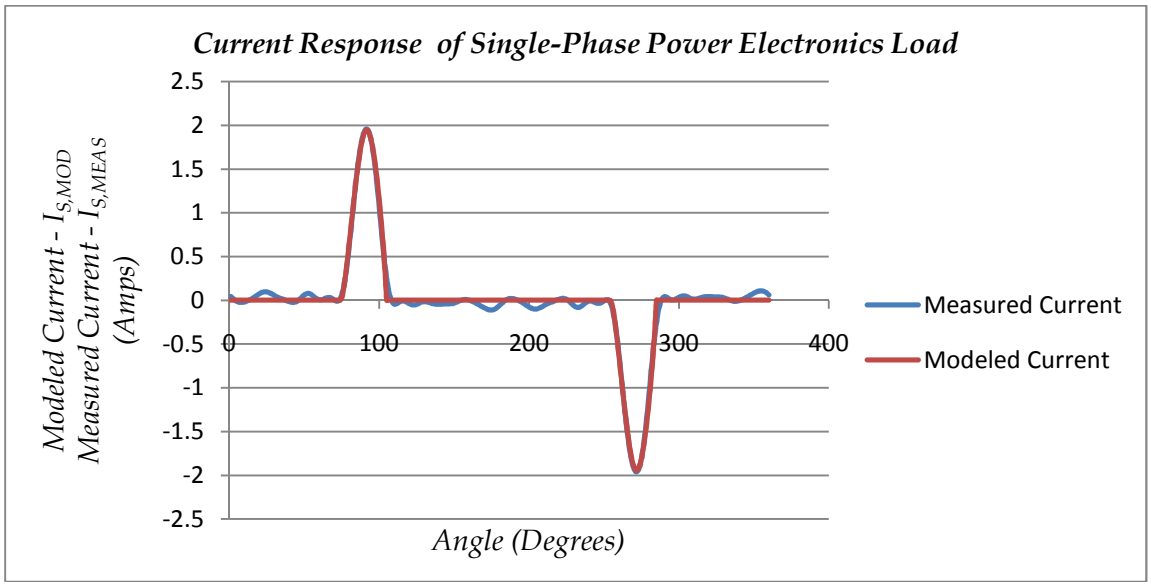
Distributed single-phase power electronics loads are usually treated as fixed harmonic current injectors in distribution system studies. Their current harmonics are characterized by harmonic Phasors $|I_h/I_1|$ $(\theta)$, where the fundamental current $I_1$ varies proportionally with the load power. The problem with the presumption of fixed harmonic current injection is that it leads to an overestimation of the resulting voltage harmonics because it neglects,

- Harmonic *Attenuation,* when several power electronics loads share common source impedance.
- Phase angle dispersion of individual current harmonics caused by variations in circuit parameters and load level; and
- Interaction between the Supply voltage harmonics and the load current harmonics.

However, the harmonic distortion affected by the proliferation of such loads exceeds any harmonic mitigation caused by the aforementioned phenomenon. Hence the term *"partial" self-compensation* is introduced as we discuss the characteristics of the single-phase power electronics loads, and the simultaneous effects of *Attenuation*, *phase-angle diversity* and the interaction between the supply voltage harmonics and the harmonic load current.

Finally, in this chapter we discuss: a) the harmonic standards that regulate the voltage and current harmonic emissions caused by the single-phase power electronics loads; b) classification of such loads according to the criteria defined by these standards; and c) the application of these guidelines.

## 2. DESCRIBING THE LOADS



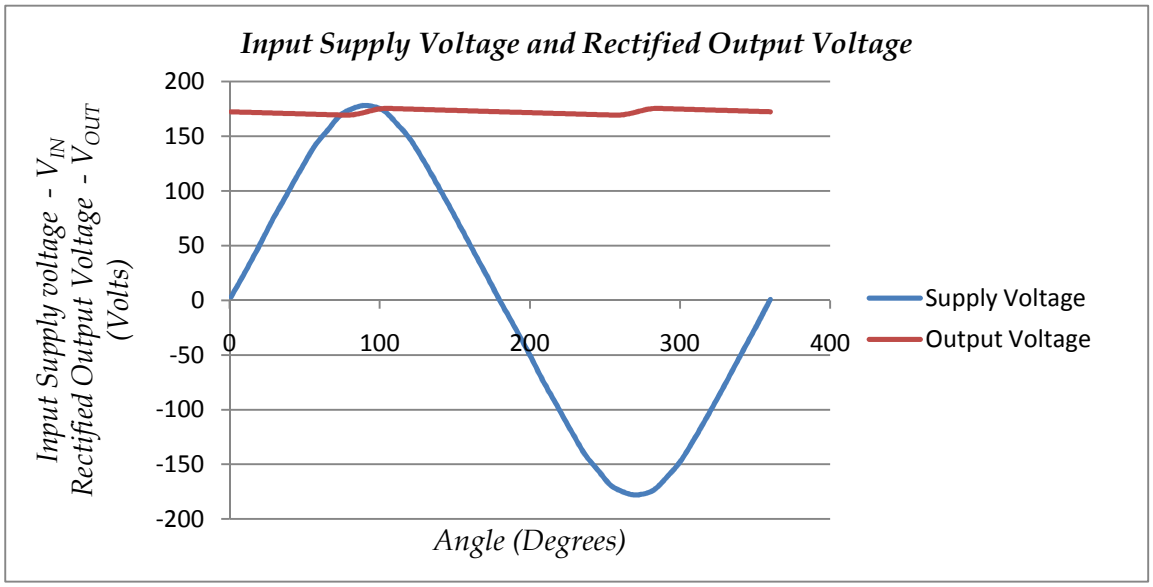




**Figure 2.1: Supply Voltage Vth (Θ), Input Current Is (Θ) and Output Voltage Vo (Θ).**

Most of single-phase power electronics loads employ a capacitor-filtered diode bridge rectifier as their power supply. The capacitor filtered diode bridge rectifier converts the AC input supply into a desired DC output. The capacitor filter or the

smoothing capacitor smoothes the DC output voltage waveform. The current and power flows from the AC side tocharge the smoothing capacitor. When not charging, the voltage across the capacitor is greater than the source voltage, but the diodes prevent current from flowing back into the AC side. Thus, the AC current and the power flow into the circuit on relatively short "bursts" or "pulses".

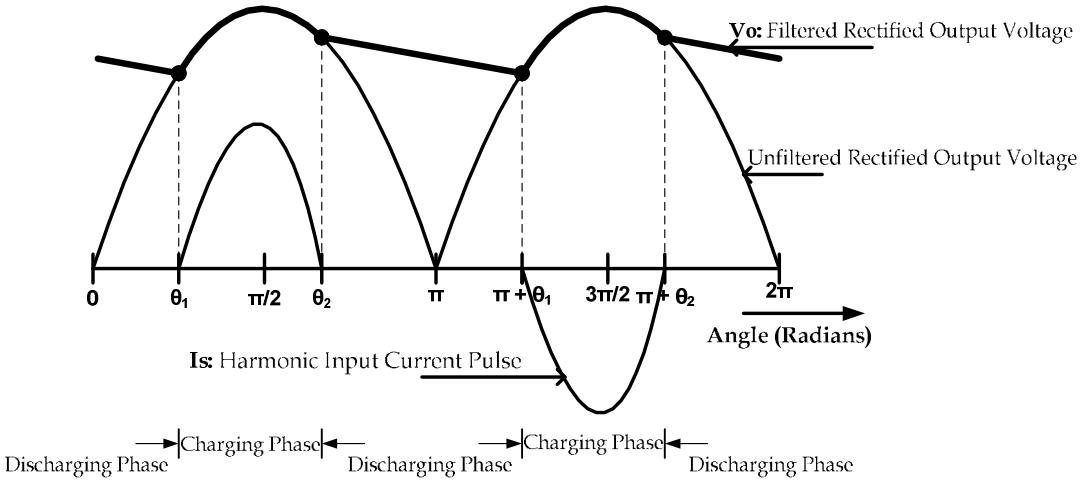



**Figure 2.2: Charging and Discharging Phase of Capacitor Filtered Diode Bridge Rectifier Circuit**

As the load power increases, the width of the current pulse becomes wider and taller; the precise shape of the current pulse depends upon the system impedance. This current is rich in harmonics and its total harmonic distortion (THDI) is in the range of 100%. The mathematical model and the harmonic analysis for the given load are described in Appendix A.

### 2.1. Effect of Load Power on the Input current harmonics (THDI)

Load Power affects the shape of the current pulse. As the Power increases, the shape of the current pulse becomes wider, taller and more skewed to the right.

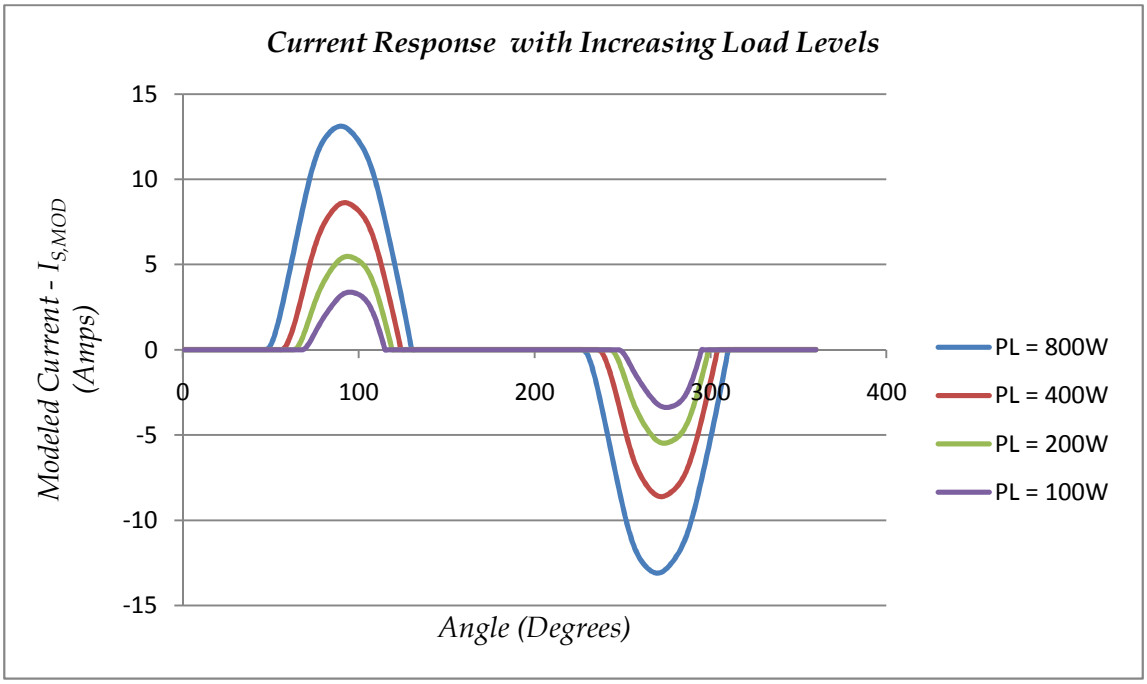



**Figure 2.3: Effect of Load Power on the Current Pulse.**

Experimentally it has been observed that as the power increases there is:

- An *Attenuation* effect on the harmonic current magnitudes (in percent of the fundamental), optimally served by a shared system impedance which leads to magnitude reductions. We can observe the effect of *Attenuation exclusively* when identical loads are connected through shared system impedance, as this minimizes the effect of *Phase Angle Diversity*. Figure 2.4 illustrates increase in *Attenuation* with increase in harmonic number.

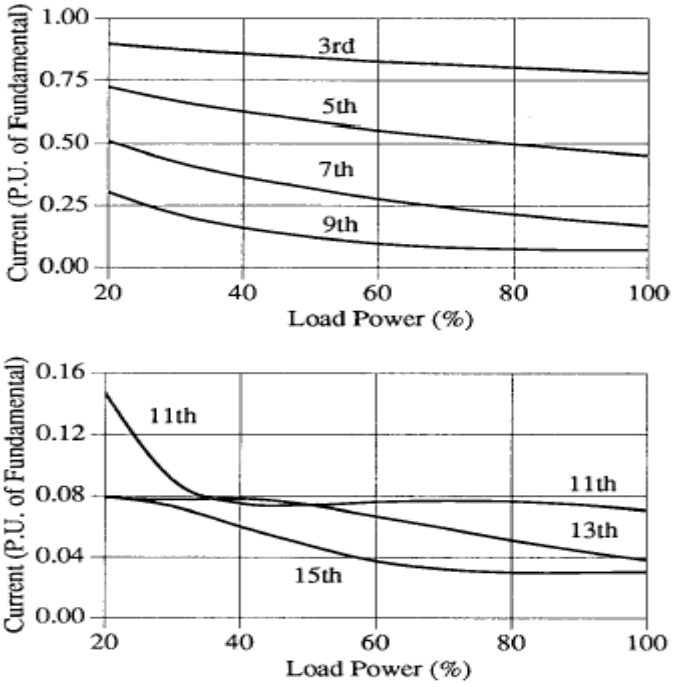



**Figure 2.4: Variations of Harmonic Current Magnitudes with Load Power**

- A significant impact on the phase-angles especially for higher-order harmonics. The phase-angle variations lead to significant cancellation due to the circulation of the harmonic currents amongst multiple loads with different power levels, especially in higher order harmonics. Figure 2.5 depicts progression of phase-angle variation with the increase in the harmonic order.

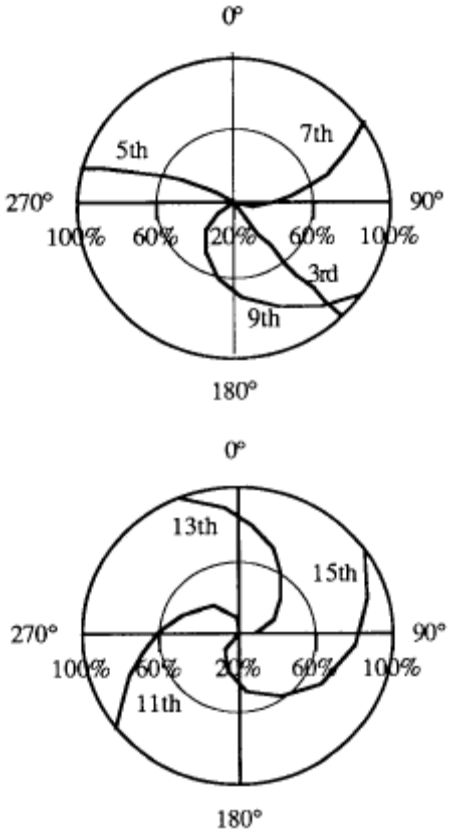



**Figure 2.5: Variations of Harmonic Current Phase Angles with Load Power**

The two phenomena, *Attenuation* and *Phase Angle Diversity* are explained in detail in the following sections:

### *2.1.1. Attenuation due to shared system impedance*

Consider the case where N identical 100W power electronic loads share a common system impedance as illustrated in Figure 2.6. In case of fixed harmonic current injection, it is customary to assume a fixed current spectrum for each load, independent of N and to apply superposition. The flaw in this technique is that it does not take into account *Attenuation*.

The term *Attenuation Factor* is defined as the ratio between the resultant current of a harmonic h for N parallel units and the arithmetic sum of currents of harmonic h from each of the N loads. This gives us a measure of the reduction of the magnitude of harmonic current due to *Attenuation*.

$$\mathbf{A^f_h = I^n_h/N^* I^1_h}$$

Where,

$I^n_h$: Resultant current for harmonic h for N units operating in parallel.

$I^1_h$: current for harmonic h when N = 1

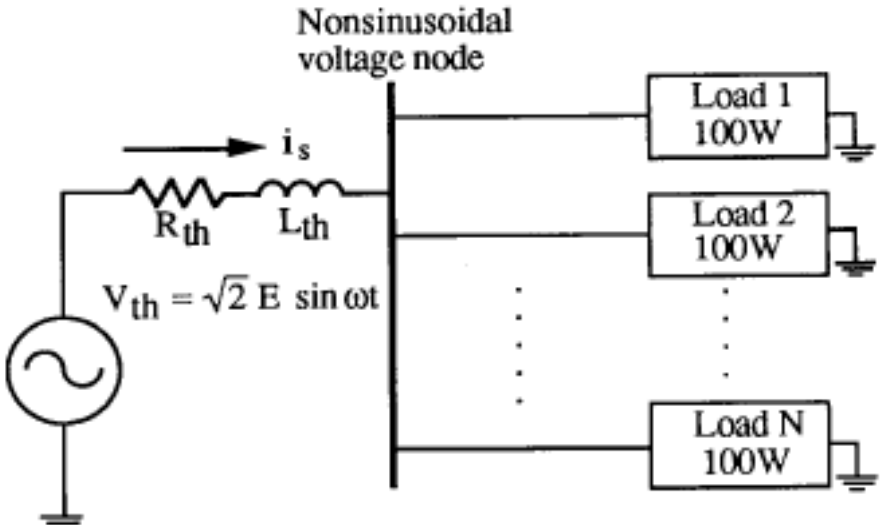



**Figure 2.6: N Identical Units with a Shared Thevenin's Equivalent System Impedance**

The resultant current flowing through the N branches is less than N times the load current flowing through a single load. The *Attenuation Factor* therefore is mostly less than one from which we can conclude that the principle of fixed current injection potentially overestimates the harmonic content in a given system.

*The Attenuation* effect is more pronounced for higher order harmonics and it tends to increase with **N**. It is observed that there is a significant attenuation of current above the 3rd multiple. However, the 3rd harmonic current, which is responsible for the most harmonic-related neutral conductor problem, experiences only slight attenuation (0.8-0.9).

There is an insignificant increase in the 13th and 15th *Attenuation Factors* as the current magnitudes tend to decrease by a factor of 1/h. Figure 2.7 illustrates the *Attenuation* effect on harmonic currents through the 15th harmonic and on the resultant THDI, due to shared system impedance.

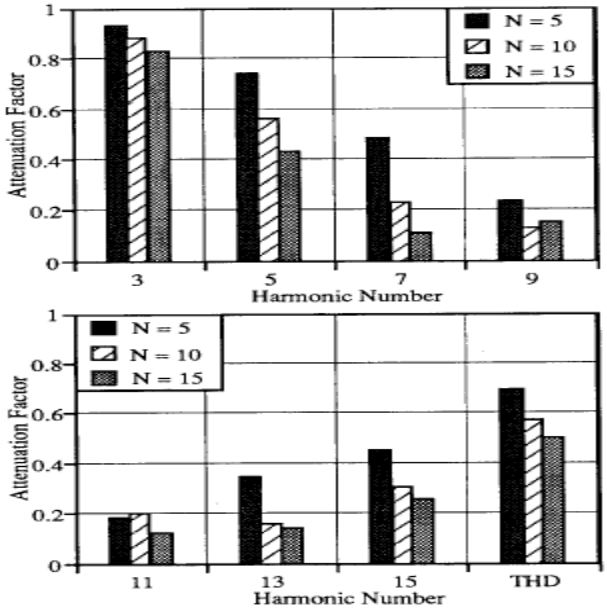



**Figure 2.7: Attenuation Factors for Harmonic Currents due to Shared System Impedance**

### *2.1.2. Diversity due to Phase-Angle variation*

Phase angle dispersion of individual current harmonics occurs mainly due to three types of variations: power level, line impedance magnitude and line impedance X/R ratio. The effect of phase-angle variations can be exclusively observed by connecting non-

identical units of loads parallel to each other with each parallel branch connected to the common "stiff" (zero system impedance) bus. By this we ensure that any harmonic cancellation is attributable only to the branch and load parameter variations.

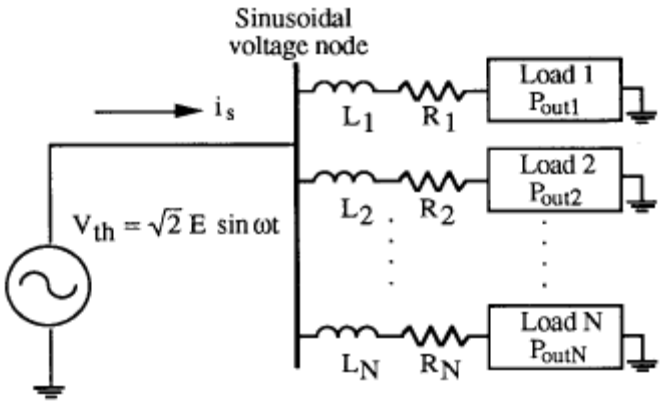



**Figure 2.8: N Identical Parallel Loads Sharing a Common "Stiff" Bus**

In order to quantify the effect of phase-angle dispersion, we define the current harmonics *Diversity Factor* as the ratio of the phasor sum of the resultant current for harmonic *h* and the algebraic sum of the current for the harmonic h flowing though each load.

$$\mathbf{Df_h} = | \sum \mathbf{I^i_h} / \sum | \mathbf{I^i_h} | |$$

Where,

i = Current load number. It ranges from 1 – N.

$I^i_h = |I^i_h| (\theta)$ = harmonic current of order h injected in the $i^{th}$ load (of the total N loads).

The *Diversity Factor* ranges between 0 and 1. A small value of $D^f_h$ implies a significant of amount of cancellation due to circulation of harmonic currents among individual loads.

The effects on the harmonic current *Diversity Factor* are dependent on the variations of circuit parameters P, Z, X/R, C, the harmonic order h, and the number of loads, N, connected to a common source. Variation of load "**Z**" has the greatest effect on the *Diversity Factor*; X/R yields similar results to P, while variation of the smoothing (discharging) capacitance C has little effect. Similarly, as the harmonic number increases, independent of any variation in the aforementioned parameters, we observe harmonic *Diversity Factor* values plummet indicating higher degree of phase cancellation. We can therefore conclude that higher order harmonics have a hightened degree of sensitivity to *Phase Angle Diversity* and the harmonic cancellation attributed to it. However, increase in the number of loads, N, connected to the Point of Common Coupling (PCC) decreases the variability of the *Phase Angle Diversity* of the harmonic current. It eventually approaches zero for very large values of N.

The following conclusions can be drawn from the individual effect of the *Phase-Angle Diversity* and *Attenuation* on the input harmonic current:

- Capacitor-filtered diode bridge-rectifier circuits, the main cause of harmonics in single-phase power electronics loads function like to fixed harmonic current injectors. However, the superposition of harmonic currents flowing through a multitude of such loads will give us an over-estimation of the harmonic content of the load current that may be measured at the mains as well as the supply-voltage harmonics that the load current causes.

- There is significant *Attenuation* of current harmonics above the 3rd harmonic multiple when a number of identical loads, such as desktop computers and television sets share common source impedance. The third harmonic experiences only slight attenuation.
- *Phase angle diversity* and the harmonic cancellation it causes is a product of four factors: individual/composite variations in load (expressed in terms of its power level); impedance magnitude; impedance X/R; and smoothing Capacitance. The 9th harmonic and beyond are the most susceptible to phase-angle cancellation. Lower order harmonics such as the 3rd and the 5th harmonics are generally unaffected by this phenomenon.

### *2.1.3. Effect of supply voltage harmonics on the total harmonic current distortion (THDI)*

Voltage distortion especially affects current distortion in cases of low order supply-voltage systems. The only time when current distortion is independent of supply-voltage distortion is when the supply-voltage is sinusoidal. Thus, in order to predict the future voltage and current distortion levels, it is necessary to investigate the effect that supply-voltage distortion will have on harmonic currents produced by these loads.

Low order supply-voltage harmonics have a significant effect on the harmonic content of the input line current (also referred to as the harmonic load current). The harmonic characteristics of the input line current are dependent on the magnitudes of the supply voltage harmonics as well as on their phase-angles.

The phase-angles of the supply voltage harmonics determine whether or not these harmonics increase or decrease current distortion. The phase-angle of a waveform indicates the shape of the harmonic waveform. For example, the 0° corresponds to a

peaking wave, wherein the fundamental and harmonic peaks are coincident, while 180° corresponds to the flattened wave, where in the negative peak of the harmonic coincides with the positive peak of the fundamental.

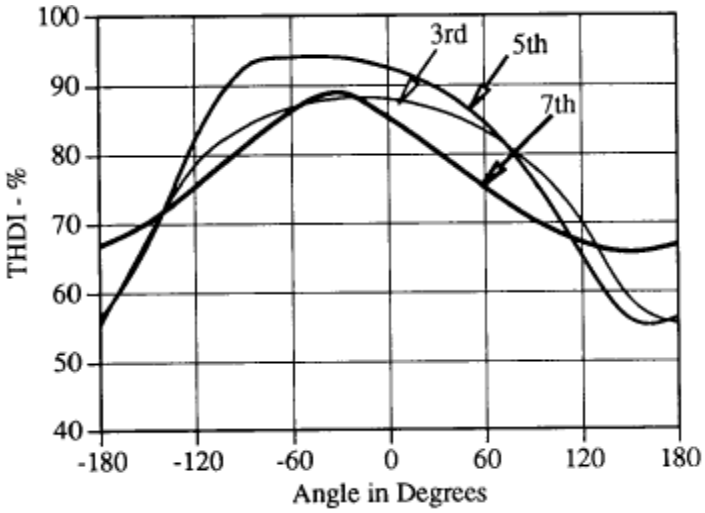



**Figure 2.9: Effect of Voltage Harmonic phase-angle on THDI**

**(0° Corresponds to Peaking Voltage Waveform and 180° Corresponds to Flattened Voltage Waveform)**

In general the peaked voltage wave increases input current distortion whereas, the flattened wave has the opposite effect as illustrated in Figure 2.9. The peaking wave yields a narrower current pulse than a flattened current pulse, as observed in Figure 2.10. Consider a single-phase 3kW, 240 V ASD heat pump with a smoothing capacitance C = 4200μF (corresponding to 6% in DC ripple voltage) and total impedance (sum of Thevenin and local line) equval to 8% (45°) (expressed on a base of 240V, 5KVA). For a 10% $3^{rd}$ voltage harmonic, for both the peaking and flattened cases, the THDIs of the current waveforms are 88% and 55% respectively. This confirms our observation about the effect supply voltage distortion has on the current distortion.

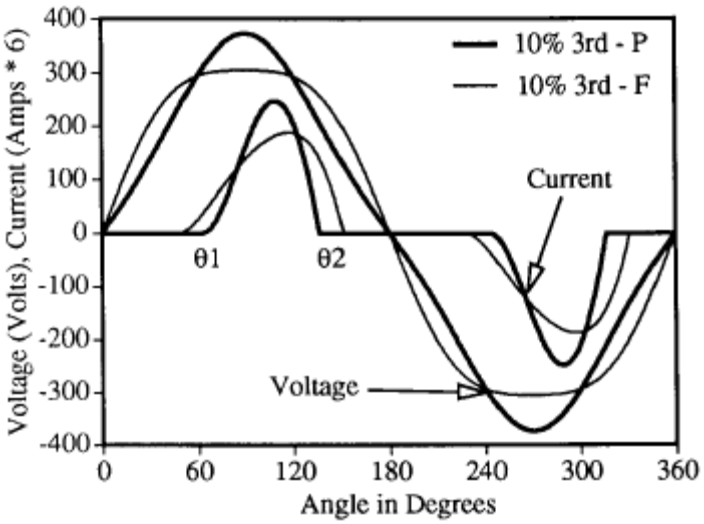



**Figure 2.10: Voltage and Current Waveforms using 10% Peaking (P) and Flattened (F) 3rd Harmonic Voltages**

It is also observed, as illustrated in Figure 2.11, harmonics above the 9$^{th}$ order have very little effect on THDI. For lower order harmonics, the difference in the THDI for the sinusoidal and non-sinusoidal case is very significant.

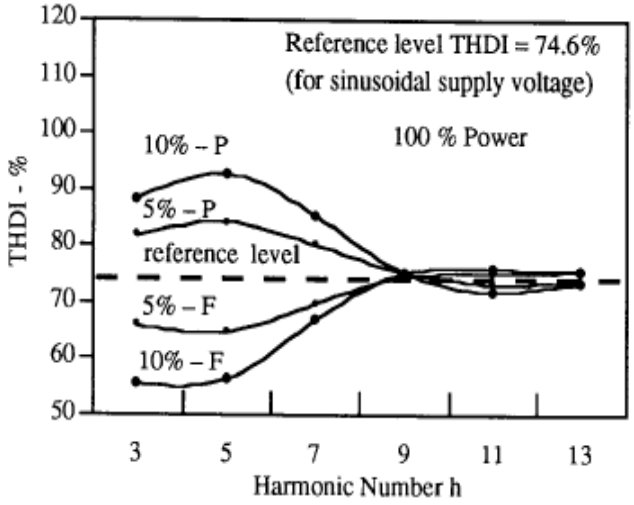



**Figure 2.11: Effect of Individual Harmonics on THDI**

#### 2.1.3.1. *Voltage Crest Factor*

The *Voltage Crest Factor* indicates whether a voltage waveform is peaking or flattened. It is a better predictor of THDI than THDV.

THDV is found by dividing the RMS value of the harmonics above the fundamental by the RMS value of the fundamental; DC is ignored. THDV lacks the phase-angle information that differentiates a peaking wave from a flattened wave. A waveform with the same THDV can be peaky or flattened. which means that we cannot use it to predict THDI.

*Voltage Crest Factor* on the other hand, defined as the ratio of the peak value of a voltage wave to its RMS value, gives a quantitative measure of how peaking or flattened the supply voltage wave form is. THDI is strongly correlated to the supply *Voltage Crest Factor* and there exists an empirical relationship between the two that is expressed in the following equation:

$$\text{THDI} = \text{m}* \text{V}^{\text{norm}}{}_{\text{crest}} + \text{b}$$

Or

$$THDI = C_1 * \log_{10}\left[\frac{Psc}{P * X/R}\right] * V^{norm}{}_{crest} + C_2 * \log_{10}\left[\frac{Psc}{P * X/R}\right] + C_3$$

Where C1, C2 and C3 are constants calculated using regression analysis on several thousand data points, by randomly varying P/Psc, X/R and THDV, yielding C1 = 159.0, C2 = -116.0 and C3 = 23.0.

### *2.1.4. Partial self-compensating effect of non-linear load currents – Attenuation due to voltage distortion*

So far we have observed the effect of supply voltage phase-angle on THDI. A peaking voltage waveform increases THDI while a flattened voltage waveform decreases THDI. In low-voltage systems, the harmonic currents produced through these loads however, have a tendency to flatten the supply voltage waveform, which again results in the reduction of THDI. However, the problem of harmonics exacerbates as the number of single-phase power electronics load proliferate offsetting any harmonic mitigation may be caused by either the supply-voltage harmonics, *Attenuation* or *Phase Angle Diversity*. This is why it is a partial effect. Figure 2.12 illustrates the partial self-compensating effect with a rising THDV and a decreasing THDI.

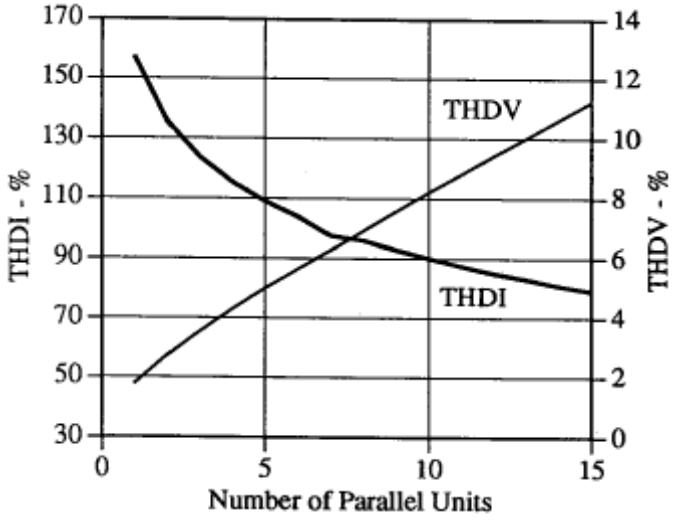



**Figure 2.12: Compensating Effect of Parallel Non-Linear Loads**

The effect of the partial self-compensation can be observed while demonstrating *Attenuation*. N identical loads are connected in parallel at the point of common coupling (PCC) sharing common system impedance. Identical loads are necessary in this set-up to

reduce harmonic cancellation due to *Phase Angle Diversity* (which is caused by variations in the load parameters and branch impedances). We can thus study the partial self-compensating effect exclusively, caused by interaction between the harmonic currents and the supply voltages. Figure 2.13 displays such an experimental set-up.

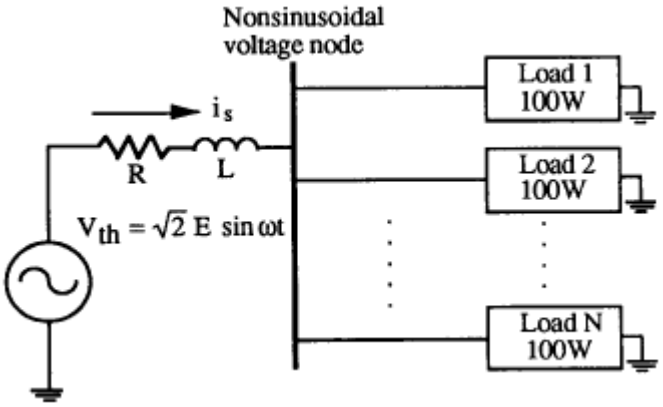



**Figure 2.13: N Identical Units with Shared Thevenin's Equivalent System Impedance to Demonstrate Partial Self-Compensation of Non-Linear Load Currents.**

We performed an experiment to demonstrate how voltage distortion and variations in system impedance affect harmonic currents in a given load that subsequently results in partial self-compensation. The experimental set-up included a single computer load with measurements taken at thirty-four different wall outlets to include the variations in system impedance. Variations in the system impedances led to variations in supply voltage distortions caused by load currents. We can draw the following observations from the experiment:

- Current Distortion (THDI) varied from 90% - 114%, with most readings between 100 – 110%.

- Voltage distortion (THDV) at the wall outlet varied from 1.4 – 3.1 %, with most readings between 1.5% and 2.5%.
- The Voltage Crest Factors of all wall output voltages were below √2, showing a definite tendency towards flattened voltage waveforms. This confirms our hypothesis that the natural tendency of the single-phase diode bridge loads currents is to create a flattened voltage which produces a self-compensating effect on current distortion.
- The phase-angle dispersion of the individual harmonic currents was not significant. Our conclusion is that the harmonic cancellation of singly-phased computer loads will occur mainly due to variation in system parameters and the different power levels of different computer models, rather than variations in branch and load circuit impedances.

### *2.1.5. Modeling the combined effect of Attenuation and Diversity*

In an actual system, non-linear loads with different operating parameters share common impedance. In effect, then, *Phase Angle Diversity* and the *Attenuation* effects should be simultaneously considered.

Hence we take into account the interactions between current distortion, and voltage distortion caused due to branch and load parameters variations, variations in system impedance and partial self-compensation simultaneously, which collectively tend to yield further "flattened" voltage waveforms and reduced current distortions.

An experiment performed to demonstrate the combined effect of *Attenuation* and *Phase Angle Diversity* confirmed the results predicted while studying these effects independently.

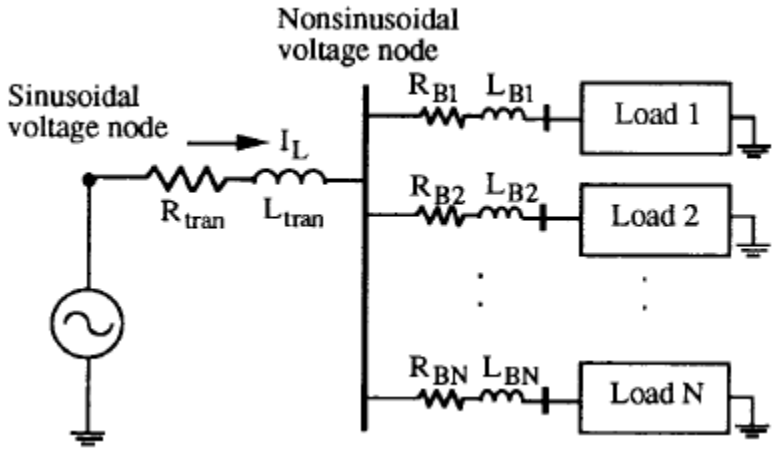



**Figure 2.14: N Branch Circuits with a Computer Loads sharing a Transformer**

The two major results of the experiment are summarized below. Together they explain the combined effect of *Attenuation* and *Phase Angle Diversity:*

- The individual current injections decrease from those of the single unit case as the system becomes more heavily loaded. The voltage distortion increases as the system loading increases,
    - The tendency of the voltage waveform is to become more flattened as the system loading increases, which in turn decreases THDI. This is due to partial self-compensation which is primarily an effect of *Attenuation*.
    - Variations in the harmonic phase-angles of individual loads also result in the net decrease of net harmonic current due to *Phase Angle Diversity* (caused by variation in branch circuit and load parameters). However, this effect is marginal compared to the harmonic cancellation due to *Attenuation*.

- The reduction in the Amps/kW induced by voltage distortion is highly dependent on system loading level; it accounts for most of the total reduction in harmonic currents.

- Harmonic cancellation due to *Phase Angle Diversity* is independent of the loading level
    - The Amps/kW reduction due to *Phase Angle Diversity* is almost constant for different load levels, where as reduction due to *Attenuation* increases substantially due to loading level.

## 3. IEC/IEEE HARMONIC STANDARDS

### 3.1. Introduction:

Most of today's information technology equipment, appliances and lighting products are classified as non-linear loads, and they utilize motor controls, power supplies and ballasts to improve cost, size, weight and/or efficiency. However, if not designed properly, the load currents these products draw from the power distribution system will still have a high harmonic content. Individually, these products are generally low power with the currents less than 16A, but their combined currents can have a significant effect. A number of these loads together can cause nuisance tripping of circuit breakers, interference with other products or fire hazards.

In order to test and limit the harmonic emissions of electrical equipment, it is necessary to study its characteristics and ratings as they influence the magnitude and nature of its harmonic emissions. The given equipment can thus be categorized into four classes A, B C, and D, based upon the abovementioned criteria of individual equipment characteristics and ratings. Furthermore, the electric equipment can be categorized into two types of harmonic sources.

Such distinctions enable us to study the characteristics of electrical equipment and thus employ the most effective means of limiting their harmonic emissions.

### 3.2. Equipment Classification and Limits:

This electrical equipment is divided into four classes based upon their voltage, current or power ratings that influence their harmonic emissions. The equipment in each class is therefore tested for harmonic emissions based upon the magnitude and nature of the emissions caused by it. Each class has a specified limit for its harmonic current emissions:

- *Class A:* It includes motor driven equipment with phase-angle control, most domestic appliances and virtually all three-phase equipment (<= 16 A). Class A is the catch-all category. Anything that does not fit into the three remaining classes is automatically categorized as Class A equipment. The limits are only defined for 230V single phase and 230/400V three-phase equipment.
- *Class B:* Includes all portable tools: Limits are 1.5 times class A.

*Note:* Class A and B limits are the easiest to meet. The pass/fail levels are fixed irrespective of the power level of the equipment being tested. Since power tools are subject to infrequent use over short periods so class B is least restrictive (1.5 times class A).

- *Class C:* Includes all lighting devices, including dimming devices, with active input power higher than 25 watts.
- *Class D:* For low power equipment having an input current with a "special wave shape" (refer Figure 2.15) and an active input power 75 → 600W. Class B, Class C and provisionally motor-driven equipment are not considered as Class D equipment.

Class D is the most controversial one as it deals with a special wave shape generated by a rectifier and capacitor filtering circuit (for example a single-phase power supply – an SMPS circuit), used in most power electronics products. The given wave shape is rich in third, fifth, seventh and so forth harmonics, and represents a low power factor to the system when the harmonics components are considered. Table 2.1 lists the harmonic current limits for Class D equipment.

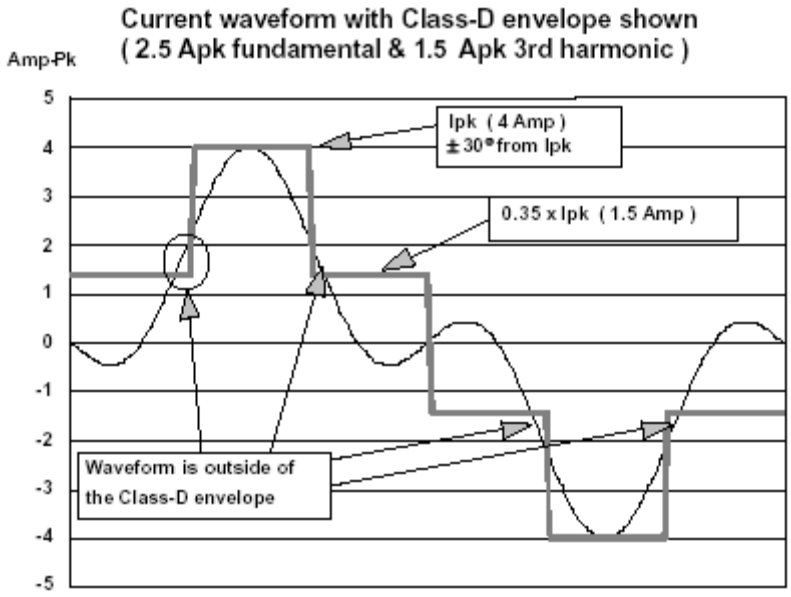



**Figure 2.15: Current Envelope that defines Class D**

IEC 1000-3-2 Limits for Class D Equipment

| Harmonic order<br>$n$ | Maximum permissible harmonic current per watt<br>mA/W | Maximum permissible harmonic current<br>A |
|---|---|---|
| 3 | 3.4 | 2.30 |
| 5 | 1.9 | 1.14 |
| 7 | 1.0 | 0.77 |
| 9 | 0.5 | 0.40 |
| 11 | 0.35 | 0.33 |
| $13 \le n \le 39$ (odd har. only) | $\frac{3.85}{n}$ | refer to Class A |

**Table 2.1: IEC 1000-3-2 Harmonic current limits for the Class D equipment**

### 3.3. Classification of Harmonic sources:

- *Voltage source converters:* The voltage source converter produces pulse-type harmonic currents with single bump wave shape for single phase systems and a double bump wave shape for three phase systems. For instance, an SMPS circuit (a single phase power supply) is a voltage source converter and so is the utility interface of a typical motor drive circuit (a three phase motor drive) is an example of voltage source converters. The steep current bump in both the circuits is caused by the charging of the capacitors.
- *Current source converters:* The current source converter replaces the smoothing capacitor by a smoothing inductor, which results in a square wave shape. A current source converter can reduce the THDI significantly but on the other hand it produces voltage spikes and notching. Such current source converters are only found in large three phase industrial equipment.

Thus based upon the above classifications, a single-phase power electronic load is a Class D device that operates like a single-phase voltage source converter.

### 3.4. Relevant harmonic standards:

Power electronics equipment such as the switch-mode power supplies, can be designed to provide the harmonic-free, unity power-factor performance. Advances in electronics, both power and control, have provided designers with new and more cost-effective options to clean up the interface with the power system. However, in most applications, the economic incentives have not been sufficient to bring about significant design improvements.

The Power system community worldwide has therefore turned to legislation and regulation to force the use of lower-harmonic electronic power supply designs. Their common objective is to preserve the sinusoidal nature of power system supply voltage while protecting power system components from harmonic current loading.

- *IEC 1000-3-2 (or EN 61000-3-2)*: The application of harmonic standards varies with different equipment size (as described in Classes A, B, C and D) and locations. Among the various IEC and IEEE harmonic standards *IEC 1000-3-2 (or EN 61000-3-2)* is best suited to the Class D single-phase power electronic load.

The IEC 1000 series deals with all the electromagnetic compliance. Part 3 sets limits and, section 2 limits harmonic current emissions for equipment input current less than or equal 16 A per phase. The number for this harmonic is derived from its predecessor, *IEC 555-2*.

*IEC 1000-3-2* sets limits for small customer's equipment, and its emphasis is on "public", "low voltage" and "households". This standard caters all four classes of equipment (Classes A, B, C and D) in the range of 220V – 415V and 0-16 A per phase.

- *IEC1000-3-4:* IEC1000-3-4 deals with individual equipment and sets limits for the whole system installation. Both single-phase and three-phase harmonic limits are addressed.
- *IEEE519-1992:* IEEE standard 519 sets limits of harmonic voltage and current at the point of common coupling (PCC). The philosophy behind this standard is to prevent harmonic currents travelling back to the power system and affecting subsequent loads and other customers. Table 2.2 lists the IEEE-519 voltage harmonic limits.

IEEE-519 voltage limits

| Bus voltage | Maximum individual harmonic component (%) | Maximum THD (%) |
|---|---|---|
| 69kV and below | 3.0 | 5.0 |
| 115kV to 161kV | 1.5 | 2.5 |
| Above 161kV | 1.0 | 1.5 |

**Table 2.2: IEEE-519 limits**

### 3.5. Proposed Harmonics Testing:

The proposed testing is based upon the requirements and conditions to set up and run a harmonic emissions test according to *EN 61000-3-2.* The given standard specifies two types of testing:

- Steady State
- Transitory (Fluctuating) State

For products with varying harmonic levels, the basic test limits are increased by 50%, but only for 10% of the testing period. Fluctuating harmonics are therefore permitted to exceed the steady state limit by 10% of any 2.5 minute test period, provided the higher 150% level is not exceeded. Fluctuating limits do not apply to Class B as these limits are already 1.5 times Class A limits.

A product should be tested with fluctuating harmonics limits if there is a question about whether the levels will vary during the test. If the measured levels do not vary, the pass-fail limits will be the same as if the steady state had been selected.

A consequence of varying harmonic levels is that a product may change classification during testing. Therefore the testing should be so performed as to change the limit classification automatically during the test.

### *3.5.1. Source Compliance Requirements*

- There are stringent requirements imposed on the power source. The voltage source should have a very low level of voltage distortion. An ideal 60 Hz sinusoidal voltage source is required to conduct compliance testing.
- not allowed to either contribute or to subtract from the current harmonic levels
- have the ability to supply widely varying currents, without causing the voltage crest factor to exceed the narrow range of 1.40 – 1.42. Other requirements include the following:
- A clean power source is required with an overall harmonic distortion < 1.25% and < 0.1% for higher harmonics from $H_{11} – H_{39}$ should be used .
- A second power analyzer is required for each phase of the power source to measure the source voltage harmonics while the test is running. In this way it is possible to demonstrate that the source met the distortion requirement throughout the test run.

### *3.5.2. Test Conditions Requirements*

- Test conditions should be selected such that the worst-case harmonics are to be evaluated.

- The harmonics test is performed for a full operating cycle of the test, which must be equal to or more than 3 seconds. For fluctuating analysis, the minimum test period is 2.5 minutes, or 150 seconds and the first 10 seconds of operation can be ignored.

# CHAPTER 3

## A New Approach –

## The *Forward* and the *Feed-Backwards* Solution

### 1. INTRODUCTION

The behavior of a single-phase power electronics load is analogous to a fixed harmonic current-injector; it injects a small quantity of harmonic current, usually 3rd and the 5th harmonics, into the main supply. A single load causes only a negligible quantity of current distortion, but as more single-phase power electronics loads proliferate, the cumulative effect of current injection into the main supply assumes significance.

A *forward* solution is, therefore, proposed to proactively predict, and mitigate effects of harmonic proliferation into the supply current due the large number of single-phase power electronics loads connected to the distribution feeder network at the point of common coupling.

In this solution, we propose an equivalent circuit model representing a distribution feeder network in the aforementioned scenario. The proposed model would simulate the harmonic conditions at the point of common coupling, and predict the harmonic supply current flowing through it. We begin pursuing this solution by creating a model for a single load connected to the distribution feeder network.

To successfully create such a model; it is imperative to ensure the accuracy of its response, while predicting the harmonic distortion of the supply current at the point of common coupling. This requires comparing and correcting the response of the equivalent circuit to a reference physical response by optimizing its circuit parameters. We call this method of correcting the response of the equivalent circuit model and determining an optimized circuit configuration the *feed-backwards* solution.

A successful *forward* solution requires an accurate equivalent circuit modelwhich we correct, verify through the proposed *feed-backwards* optimization solution.

*Problem Definition*

The circuit of a single-phase power-electronics load entails a single-phase capacitor-filtered diode bridge rectifier that is connected to a resistive load, as shown in Figure 3.1. Powered by the 60 Hz 120 VAC supply and composite system impedance that connects them, the rectifier circuit converts the AC voltage into a rectified DC voltage that forms the input to the single-phase power electronics load. It is the component primarily responsible for the harmonic current generated in an individual load.

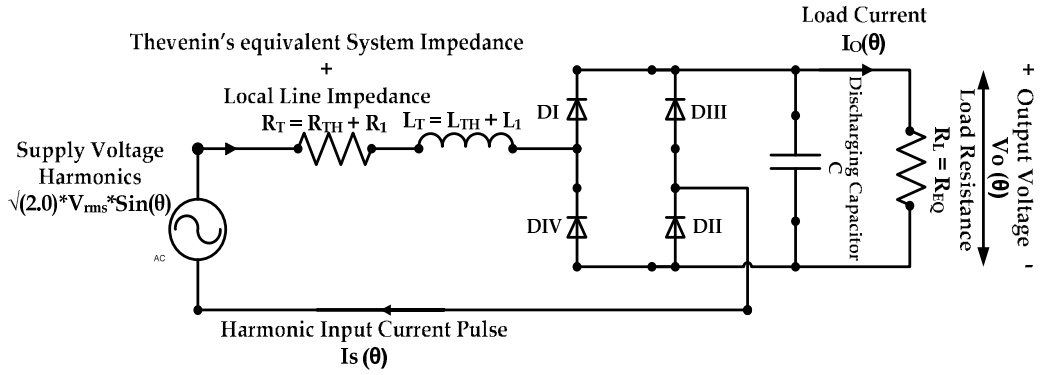



**Figure 3.1: Single Phase Diode Bridge Rectifier Model**

The composite system impedance of the circuit is a series combination of the Thevenin's equivalent impedance of the voltage source, impedance of the shared-transformer that connects all loads to the point of common coupling, and the resultant branch impedance of N single-phase power electronics loads connected to the point of common coupling through N parallel circuits. Mathematically the system impedance is expressed as,

$$Z_T = (R_{TH} + R_{TRAN} + R_B) + j\omega(L_{TH} + L_{TRAN} + L_B)$$

Or,

$$Z_T = R_T + j\omega L_T \ldots (1)$$

Figure 3.2 illustrates the configuration of N single-phase power electronics loads connected at the point of common coupling to a sinusoidal voltage source via a shared-transformer.

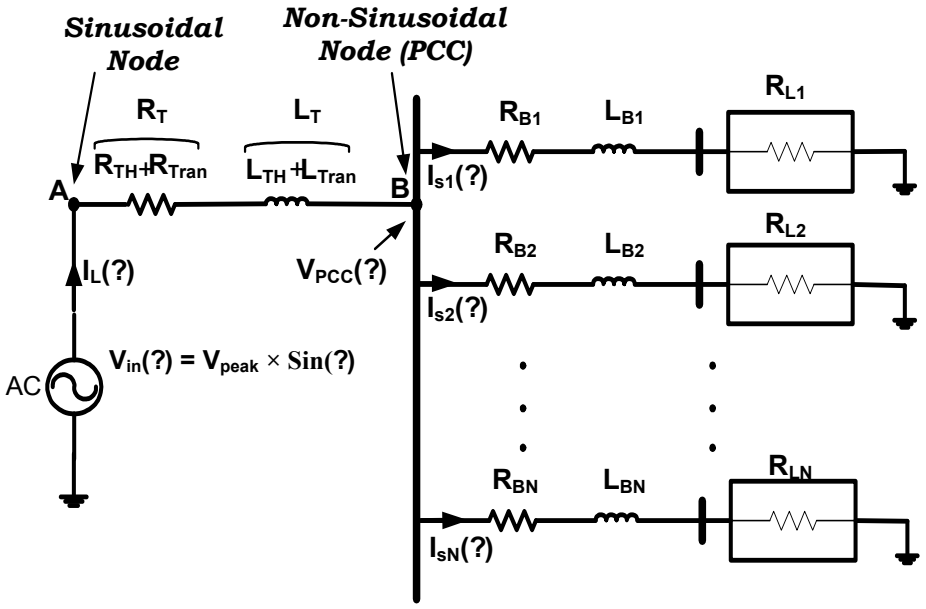



**Figure 3.2: N Single-Phase Power Electronics Loads Connected at the PCC**

An input current pulse $I_S$ flows in the diode bridge-rectifier circuit of an individual load during its charging phase. The product of the current $I_S$ and the collective non-linear system impedance, $Z_T$, creates a harmonic potential, $V_{PCC}$, at the point of common coupling.

Applying KCL at the PCC, we surmise that the current through the main supply is the sum of individual load currents (or the individual input current pulses) $I_L$, such that,

$$I_L = \sum_{N\ Loads} I_{S,N} \ldots (2)$$

As the number of loads connected to the PCC increases, individual current pulses, $I_{S,N}$ add to the main supply current $I_L$, exacerbating the harmonic content of both $V_{PCC}$ and $I_L$. Conversely, the harmonic distortion of $V_{PCC}$ aggravates the harmonic content of a current $I_{S,N}$ flowing through an individual load N.

The THDV at the PCC varies within the range of 2-5%, well within the tolerance limit; but as levels of voltage distortion increase, the THDI of the load current $I_S$ is amplified up to 40%. Such amplified current distortion levels can cause significant damage to all loads connected to the distribution feeder network.

*Proposed Solution* – The *forward* solution

We proposed a circuit model suitable for predicting the current that results from a thousands of loads connected to the distribution feeder network. This model will have the ability to simulate harmonic conditions at the point of common coupling, which would enable it to predict the harmonic distortion in supply current flowing through the PCC. It is a significant tool in mitigating harmonic distortion in the supply current at the point of common coupling. It allows us to perform compliance tests by ensuring that the harmonic current at the PCC, as a response to a pure 60 Hz sinusoidal supply voltage, remains within the within the prescribed harmonic limits.

In order to perform harmonics mitigation analysis at a distribution-feeder network, we must consider the collective harmonic impact of all single-phase power electronics loads connected to the distribution feeder. We proposed an equivalent circuit model – an aggregation of all single-phase power electronics loads connected at the point of common coupling is proposed. Such a model simulates all harmonic current-injectors collectively as a single source, and combines their individual contributions as a single composite harmonic signal. This constitutes the *forward* solution.

The configuration of this equivalent circuit is identical to the circuit configuration of just one load connected to the distribution feeder network. The parameter values that define the circuit may vary, as they are contingent upon such factors, as the number of loads connected to the network, the nature of these loads, the variations in the harmonic content of the supply voltage, the X/R ratio, Phase-shift variation etc.

*Deriving the Model Response*

The response of an equivalent circuit model is based upon the operating principle of the diode bridge-rectifier circuit. We write the mathematical expression of the response of the equivalent circuit in terms of the input current pulse, $I_{S,MOD}$, flowing through the rectifier circuit. $I_{S,MOD}$ is a function of the input supply voltage $V_{IN}$, the circuit parameters – discharging capacitance $C$, load resistance $R_L$, and equivalent system impedance, $Z_T = R_T + j\omega L_T$. The complete derivation of the modeled response is detailed in Appendix A.

*Validating the Model and its Response* – The *feed-backwards* solution

The next logical step after generating the equivalent circuit model is to validate the model by verifying the accuracy of its response. The response of the equivalent circuit model is measured in terms of the input current pulse $I_{S,MOD}$ which is an aggregate of the individual current pulses of $N$ individual loads connected to the PCC. Mathematically, this relationship is expressed as:

$$I_{S,MOD} = \sum_{N\ Loads} I_{S,N} \ldots (3)$$

Comparing equations 2 and 3, we infer that $I_{S,MOD}$ is equivalent to the main supply current $I_L$.

The degree of accuracy of the simulated response of the analytical model is judged by how closely it replicates the physical response; optimization of the simulated

response constitutes a *feed-backwards* solution that validates the circuit. For some input input voltage, we compare the simulated current response, $I_{S,MOD}$, for the equivalent circuit to its physical equivalent $I_{S,MEAS}$, reducing the difference between the two by varying the circuit parameters, $C$, $R_L$ and $Z_T$, until we reach the point at which the simulated response replicates the physical response. We call this unique combination of parameters the *Correction Factor* that generates the optimized simulated response.

We employed an experimental apparatus, the *Harmonics Testing Station, which was* designed and developed in our laboratory to validate the proposed analytical model of the equivalent circuit. A LabView based platform, it compares and corrects distortion levels of voltage measured at the point of common coupling against the main reference supply-voltage.

In essence, the *Harmonics Testing Station* is the experimental equivalent of the proposed analytical model. It simulates the conditions at the PCC with N single-phase power electronics loads connected to it. The model is considered valid if the analytical model, for a given voltage input generates a theoretical response, $I_S$, and a unique *Correction Factor* that is consistent with the harmonic response of the multiple single-phase power electronics loads connected to the testing station.

*Application of the Model*

The ability to perform a theoretical harmonic analysis at the point of common coupling, offers us an ability to predict the extent of harmonic amplification in a network, prior to its actual occurrence. By extension, it will also help us determine the effect of harmonic distortion in the supply voltage on main supply current and vice-versa. This offers us a significant advance in monitoring and proactively containing harmonic

regression of the voltage at the PCC, and the main supply current in a real physical scenario.

Additionally, such a model will allow us to theoretically conduct the compliance tests prescribed for *IEC 1000-3-2* for Class D equipment, with any available supply voltage and then correcting the response of the equivalent circuit model for a pure 60 Hz sinusoidal supply voltage (as required by the testing criteria set by IEC).

## 2. MATHEMATICAL FORMULATION OF THE PROBLEM AND ITS PROPOSED SOLUTION

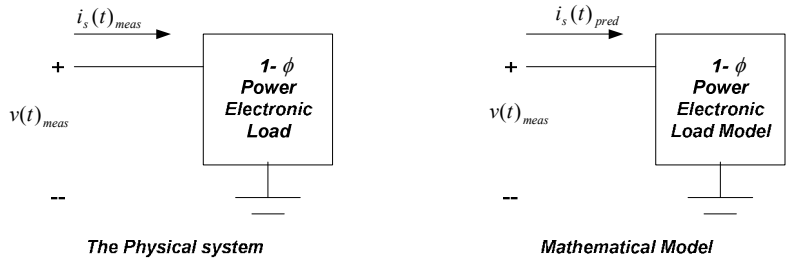



**Figure 3.3: Representation of the physical system and its analytical model of its Equivalent Circuit**

A mathematical model of a single-phase power electronics load is derived and analyzed with the purpose of emulating the system response of a load powered by a sinusoidal voltage supply, $V_{IN}(t)$[2], at the PCC. Mathematically, the supply voltage is expressed as:

$$V_{IN}(\theta) = \sqrt{2.0}\sum_N E(n) \times Sin\big(n\theta + \emptyset(n)\big) \ldots (4)$$

Where, $\theta = \omega t$

The circuit configuration of one load connected to the distribution feeder network at the point of common coupling is identical to equivalent circuit model for N loads connected to the same node. Thus, the mathematical model derived for a single circuit is

[2] $V_{IN}(t)$, $V_O(t)$ and $I_S(t)$ are time-varying signals and are therefore expressed explicitly as functions of time.

applicable to the equivalent circuit model for multiple loads. However, the parameter values that define the circuit may vary as they are sensitive to the number of loads connected to the network, nature of such loads, and variations in the harmonic content of the Supply Voltage, the X/R ratio, Phase-shift variation etc.

The analytical model for an equivalent circuit of *N* aggregated single-phase power electronics loads (illustrated in Figure 3.1) connected to the point of common coupling can be described in terms of its load current $I_{S,MOD}(t)$ and load voltage $V_{O,MOD}(t)$. $I_{S,MOD}(t)$ and the load voltage $V_{O,MOD}(t)$ are a function of the following parameters that define the equivalent circuit model of a single-phase power electronics load:

- $R_L$ → Resistive load connected across the Diode Bridge rectifier circuit;
- $C$ → Discharging Capacitance;
- $R_T$ → Real component of the composite system impedance of the equivalent circuit; and

  $L_T$ → Reactive component of the composite system impedance of the equivalent circuit

For a detailed derivation of the mathematical model, refer Appendix A. $I_{S,MOD}(t)$ and $V_{O,MOD}(t)$ are expressed in terms of their Fourier Coefficients as:

$$I_{S,MOD}(t) = \sum_{\substack{k=1 \\ k=odd}}^{N} \left(a_{k,MOD} \cos(k\omega_O t) + b_{k,MOD} \sin(k\omega_O t)\right) \ldots \quad (5)$$

$$V_{O,MOD}(t) = \sum_{\substack{k=1 \\ k=odd}}^{N} \left(c_{k,MOD} \cos(k\omega_O t) + d_{k,MOD} \sin(k\omega_O t)\right) \ldots \quad (6)$$

Where,

$k$ → 1,3, 5, 7 . . . .up to the 25$^{th}$ harmonic.

$a_k$, $b_k$, $c_k$ *and* $d_k$ → Fourier coefficients corresponding to each harmonic k.

The model derived is valid, if both the physical and the predicted models, powered by the same supply-voltage $V_{IN}(t)$, and expressed in terms of the currents $I_{S,MEAS}(t)$ and $I_{S,MOD}(t)$ respectively, generate a near-identical response. Error between $I_{S,MEAS}(t)$ and $I_{S,MOD}(t)$ can be expressed as the difference between their Fourier coefficients as shown in equation 7[3],

$$Error = \sum_{\substack{k=1 \\ k=odd}}^{N} \left[ \left(a_{k,MEAS} - a_{k,MOD}\right)^2 + \left(b_{k,MEAS} - b_{k,MOD}\right)^2 \right] \ldots (7)$$

Where,

$$I_{S,MEAS}(t) = \sum_{\substack{k=1 \\ k=odd}}^{N} \left(a_{k,MEAS} \cos(k\omega_O t) + b_{k,MEAS} \sin(k\omega_O t)\right) \ldots (8)$$

To correct the modeled response, $I_{S,MOD}(t)$ so that it replicates the physical entity $I_{S,MEAS}(t)$, the aforementioned parameters are varied until the difference, *Error*, between them is minimized for a unique combination of parameters $R_L$, $C$, $R_T$, and $L_T$. The determination of this unique solution of the given parameters is the *Correction Factor* that validates the mathematical model.

Hence, a *feed-backwards* method is developed using a known (and desired), measured response as a reference to determine the circuit parameters of an equivalent model that would generate such response. This method, for an initial estimate of the circuit parameters, executes the response of the equivalent circuit model; it continuously corrects its theoretical response to a final consistent, and robust optimized circuit configuration, despite variations in physical conditions it simulates at the distribution feeder network. This *feed-backwards* optimization method takes form of *Response*

[3] The algorithm to calculate the difference between the two currents employs the sum of differences between the current values at each degree of a 360 degrees cycle, though both methods are valid. The method of determining the difference in harmonic coefficients is used to visually assess the extent of optimization of the modeled response.

*Optimization* algorithms. The success of the *feed-backwards* method is determined in the consistency of the optimized parameter solution.

### 2.1. Execution of the Model:

The *Response Optimization* algorithms determine the shortest path to optimization of an equivalent circuit model that accurately represents the conditions at the point of common coupling connected to a multitude of single-phase power electronics loads. The *feed-backwards* method contains three stages – *Response Generation, Response Comparison* and finally, *Response Optimization*.

- Response Generation involves executing the response of the equivalent circuit model for a set of circuit parameters, $C$, $R_L$, $R_T$, $L_T$, powered by harmonic voltage source.
- Response Comparison quantifies the difference between the measured reference response and the theoretical response of the equivalent circuit model. This difference is used to assess the extent to which optimization has been achieved through continuous correction of the simulated theoretical response.
- Response Optimization is an iterative process in which the theoretical response of the equivalent circuit model is optimized by varying its circuit parameters, until simulated response matches the physical reference. This algorithm employs Response Generation and Response Comparison to measure the optimization achieved at every iteration.

### 2.2. Application of the model:

Our proposed equivalent circuit model is generated by means of this *feed-backwards* method. This model, in turn, delivers our *forward solution* of computing harmonic currents produced by single-phase power electronics loads connected at the

point of common coupling. The equivalent circuit model, once developed, would allow us the following capabilities:

- Enable harmonic mitigation analysis at the point of common coupling. The equivalent circuit would allow us to predict the harmonic content of the voltage at the point of common coupling, the main supply current, and even estimate the harmonic content in the individual loads connected to the system. Such prior knowledge would allow us to take proactive harmonic mitigation measures.
- Verify the phenomenon of *attenuation, phase-diversity* and the resulting *partial self-compensation* of the main supply current $I_L$, through the flattening supply voltage at the PCC.
- Perform compliance tests prescribed in *IEC 1000-3-2* for Class D equipment, using any available supply-voltage, and in particular, a sinusoidal supply voltage (as required by the testing criteria set by IEC). This would enable us to estimate the worst-case voltage distortions while still ensuring that the current distortion stays within the standards prescribed by *IEC 1000-3-2*.
- Successfully derive and model other loads such as Microwave ovens and Compact Fluorescent Lights (CFLs) in much the same way as single-power electronics loads.

## 3. MODEL AND PROCEDURE VALIDATION USING THE HARMONICS TESTING STATION

The *Harmonics Testing Station* is a Lab View based system that can power a load with a *Target V* voltage of a known harmonic content. The harmonic content of *Target V* consists of individual harmonics through the $25^{th}$ multiple of 50/60 Hz. In some cases, a perfect sine wave (with zero harmonics) is desired.

The testing station is an experimental apparatus designed with the explicit purpose of conducting harmonic analysis at the point of common coupling, with a multitude of single-phase power electronics loads connected to it. It simulates voltage that appears at the point of common coupling (PCC) as the voltage gradient, *Load V,* across a load (or multiple loads) connected at the PCC, as shown in Figure 3.4.

*Load V,* therefore, is analogous to the voltage at the point of common coupling that appears across each load. The ratio of *Load V* to the branch and load impedance generates an individual load current, $I_{L,MOD}$ that flows through the branch connecting that load. Individual load currents add up to constitute the main supply current $I_L$ (as illustrated in Figure 3.2) at the point of common coupling.

A feedback correction procedure implemented in the testing station corrects *Load V* to match its harmonic content to the user-defined voltage reference, *Target V* analogous to correction of the simulated response of the equivalent circuit model to the reference physical response described above.

In the *Harmonics Testing Station*, $I_L$ is the current that flows through the testing station before its divides itself into several load-carrying branches, which are all connected at a node representing the point of common coupling. The testing station determines the reference physical response, $I_{L,MEAS}$ of the equivalent circuit as the ratio of the reference voltage *Target V* to the combined system impedance. For successful harmonics compliance testing purposes, *Target V* is a 60 Hz sinusoidal voltage.

Based upon its operating principle, the testing station, we can be view the experimental equivalent of the proposed analytical model for a multitude of single-phase power electronics loads, all connected to a point of common coupling and powered by a sinusoidal harmonic voltage source. The model is considered valid if it generates a

theoretical response $I_{L,MOD}$ and a unique *Correction Factor* consistent with the response of multiple single-phase power electronics loads connected to the testing station and powered by an identical supply voltage.

This *Harmonics Testing Station*, therefore, is an ideal choice to verify and validate the proposed equivalent circuit model and its operation. Finally, the testing station also has the ability to demonstrate the effect of *attenuation* and *partial self-compensation*.

### 3.1. Modeling Testing Station and its Representation of the System at the Point of Common Coupling (PCC)

The Testing station is set up to represent a system of multiple single-phase power electronics loads connected at the point of common coupling (PCC). It can be used to determine the voltage distortion caused at the PCC due to the interaction between the harmonic load current and the system impedance.

Under no-load conditions, the voltage at the PCC is undistorted and contains the desired harmonic content. When single/multiple units of load are connected in parallel at the PCC (refer to Figure 3.2), harmonic currents flow through each load (each being expressed as the ratio of voltage at the PCC and its corresponding non-linear load impedance). The sum of these harmonic currents yields the harmonic load current $I_L$, which flows through the system impedance. Product of the load current $I_L$ and system impedance causes voltage distortion at the PCC. Mathematically, it is represented as

$$V_{PCC} = I_L \times Z_T \ldots (9)$$

Also,

$$Load\ V = V_{PCC} \ldots (9)$$

For this reason, the voltage at the PCC, labeled as *Load V*, deviates from its desired value, *Target V,* and its harmonic content. A basic block diagram of the Testing Station is illustrated in Figure 3.4.

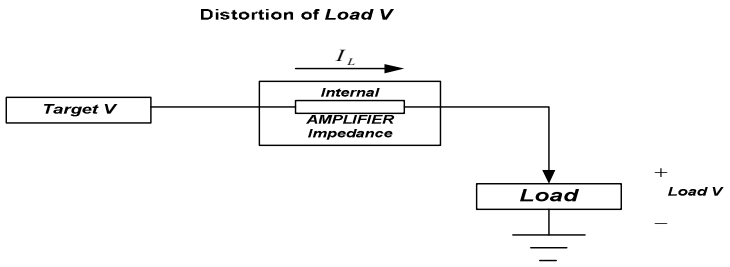



**Figure 3.4: Load V Distortion without Feedback**

## 3.2. Validation of the Mathematical Model through Testing Station and Development of the Correction Factor

Corrective feedback measures have been developed and employed as a part of the Testing Station apparatus to modify *Load V* and match it to the user-defined desired voltage *Target V*.

The process of harmonic optimization of *Load V* involves calculating the difference between its harmonic coefficients and those of reference signal *Target V*. The *"worst harmonic offender"* – a term used for the harmonic that entails the greatest difference between the two signals, is identified. A signal equal in magnitude and inverse of this harmonic difference is added to the harmonic spectrum of the *Load V* signal. It eliminates the *"worst harmonic offender"* and the corresponding highest individual harmonic difference between the two signals. We eliminate other individual harmonic differences are eliminated in this manner as well continuing until we are sure the *Load V*

signal is optimized. The optimal signal is achieved when the *Load V* harmonic content matches that of *Target V,* within acceptable limits of accuracy.

As we explained in the last section, comparing *Load V* against a desired voltage *Target V* is equivalent to comparing the simulated current pulse $I_{S,MOD}$ (the ratio of *Load V* and system impedance) and the $I_{S,MEAS}$ (the ratio of *Target V* and system impedance).

We verify the equivalent circuit model through comparison and optimizationof the equivalent circuit model by providing evidence of a unique solution of optimized parameters or a *Correction Factor.* This simulates and predicts an accurate harmonic response at the PCC, for multiple single-phase power electronics harmonic current injectors connected to the Testing Station.

An experiment, with a composite load connected to a harmonic voltage source is simulated by connecting that load to the *Harmonics Testing Station* with an identical voltage supply. The results of the experiment prove the accuracy of the equivalent circuit model in terms of its response, the input current pulse $I_S$. These results also demonstrate the utility of the *Harmonics Testing Station* as a benchmarking tool with regard to the the response of the proposed equivalent circuit model.

# CHAPTER 4

# Understanding the *Feed-Backwards* Method

## 1. INTRODUCTION

In Chapter 3, we established the usefulness of a *feed-backwards* method for determining a correct optimized circuit configuration (*Correction Factor*) of the equivalent circuit model. Subsequently, an optimized circuit model forms the basis of a *forward* solution that predicts the harmonic response for a multitude of single-phase power electronics loads connected at the point of common coupling. In the following chapter we will explain the *feed-backwards* method of optimization and how it can be used to solve the harmonics problem.

Mostly, harmonic distortion at a distribution feeder network can be attributed to a multitude of single-phase power electronics loads connected at the point of common coupling (PCC). Each power-electronics device, in effect, operates like a fixed harmonic current injector; a single load does not affect significant harmonic distortion in the main supply, but collectively their impact cannot be ignored.

Each single-phase power electronics load, for modeling purposes, is connected through a dedicated branch, with branch impedance $Z_B = R_B + j\omega L_B$. All branches connect at a common node, the PCC, and subsequently to the supply voltage through a common shared-transformer. Figure 4.1 illustrates N parallel loads connected between the PCC (node B) and the ground.

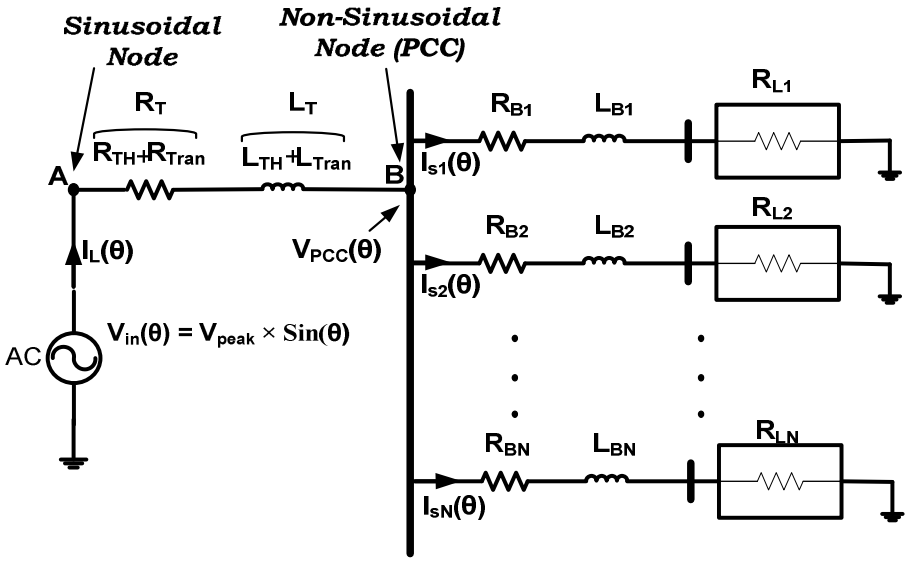



**Figure 4.1: N Single-Phase Power Electronics Loads Connected to the Point of Common Coupling**

When the current $I_S$, flowing through a given load is injected back into the main supply, it will cause an infinitesimal increase in the harmonic content of the main supply current, $I_L$. As current $I_S$ while flows through a given branch, it interacts with the non-linear branch impedance, ($R_B + j\omega L_B$) and resistive load impedance, $R_L$ and develops a harmonic potential, $V_{PCC}$, at node B. Mathematically, the harmonic potential, $V_{PCC}$, is expressed as:

$$V_{PCC}(\theta) = I_S \times (R_B + j\omega L_B + R_L) = I_S \times Z_B$$

An ideal sinusoidal voltage source is connected at node A. The current $I_L$ flows between the nodes A and B through the impedance of the voltage source denoted by its Thevenin's equivalent $Z_{TH} = R_{TH} + j\omega L_{TH}$, and the non-linear impedance, $Z_{TRAN} = R_{TRAN} + j\omega L_{TRAN}$, of the shared transformer. Mathematically, the main current supply can be expressed as,

$$I_L(\theta) = (V_A - V_B)/(Z_{TH} + Z_{TRAN})$$

$$I_L(\theta) = \big(V_{IN}(\theta) - V_{PCC}(\theta)\big)/(Z_{TH} + Z_{TRAN})$$

Other single-phase power-electronics loads contribute to the harmonic content of the main supply current as well. As the number of loads connected to the distribution feeder network increases, it exacerbates the harmonic content of the voltage, $V_{PCC,}$ developed at the PCC. Consequently, the harmonic voltage developed across the Thevenin's equivalent impedance (due to its interaction with load current $I_L$) will add to $V_{PCC}$ and exacerbate the harmonic content of the main supply voltage. In mathematical terms,

$$V_{IN}(\theta) = I_L(\theta) \times (Z_{TH} + Z_{TRAN}) + V_{PCC}(\theta)$$

$$V_{PCC}(\theta) = \sum_{N\ Loads} \Big(I_{S,N}(\theta) \times \big(R_{B,N} + j\omega L_{B,N} + R_{L,N}\big)\Big)$$

This is a cyclical process in which an increase in harmonic distortion in the supply voltage will result in an aggravation of the harmonic content of the supply current $I_L$ and subsequently of the potential $V_{PCC}$. At the same time, however, we also observe a phenomenon of *PartialSelf-Compensation*. An increase of harmonic distortion in the supply voltage will be accompanied by a flattening of its sinusoidal curve. A flattened voltage waveform in turn tends to alleviate the current distortion, especially the 3$^{rd}$ and the 5$^{th}$ harmonics. Together, these harmonics account for most of the harmonic reduction. While reduction in the harmonic content of current $I_L$ will tend to flatten the voltage waveform further, the net voltage and current distortion will still increase as more power-electronics loads proliferate. However, we risk over-estimating harmonic distortion of the current if we ignore partial self-compensation [3].

In conclusion, the net harmonic distortion of the supply voltage, and current increases with harmonic proliferation, and its severity affects all the loads connected at that distribution network.

In order to perform harmonics analysis at a distribution-feeder network, we must consider the collective harmonic impact of all single-phase power electronics loads connected at the distribution feeder. We need to design an equivalent circuit model – an aggregate of all single-phase power electronics loads connected at the point of common coupling. Using this model, we can simulate all harmonic current-injectors collectively as a single source, and combine their individual contributions as a single composite harmonic signal. Figure 4.2 illustrates such a circuit model.

The equivalent circuit model in its final circuit configuration is as applicable for a single load connected to the distribution feeder, as it is relevant to N loads connected to the network. The circuit configuration remains the same, although the parameter values that define the circuit may vary based upon the number and nature of loads connected to the network. The circuit parameters are also sensitive to the harmonic variation in the input supply voltage, phase-shifts, the X/R ratios etc.

Therefore, our proposed circuit model, ought to include an AC voltage source with user-defined harmonic content that represents the voltage at the point of common coupling, elements of a diode bridge rectifier circuit – discharging capacitance $C$, system impedance expressed collectively as $Z_T = R_T + j\omega L_T$, wiring or branch impedance $Z_B = R_B + j\omega L_{B1}$; and Load Resistance $R_L$. By matching the simulated response, expressed in terms of the input current pulse $I_S$, to an actual physical response, we establish the validity of our model. The equivalent circuit model is said to be valid if, for a particular combination of the circuit parameters $C$, $R_L$ and $Z_T$, known as the *Correction Factor*, the

simulated response replicates the physical response of the system accurately. Thus, it will accurately predict the harmonic response generated at a distribution feeder network, with thousands of single-phase power electronics harmonics-injecting sources connected to it.

In chapter 4, we will derive an analytical model for the equivalent circuit, and a mechanism to generate the parameters of the equivalent circuit using that model such that the simulated circuit response matches its physical response accurately. This analytical model is a mathematical expression written in terms of the input current pulse $I_S$, and the rectified output voltage $V_O$, which is how we represent the equivalent circuit. A *Load Response* algorithm is created to execute the analytical model. It entails simulating the response of this circuit. The response of a single-phase power electronics load connected to a sinusoidal voltage supply is expressed in terms of input current pulse $I_S$. For future references, the simulated current pulse is now denoted as $I_{S,\,MOD}$ while the actual physical response is expressed as $I_{S,\,MEAS}$.

The difference between the simulated and the physical response of the system is determined using an *Error Calculation* algorithm. It is measured as the difference between the currents, $I_{S,MEAS}$ and $I_{S,MOD}$. This difference can either be determined as the sum of differences between the values of two current pulses, calculated for each degree in a 360-degrees cycle, or it can be expressed as the difference between the harmonic (Fourier) coefficients of the two current pulses. The *Error Calculation* algorithm uses the former mechanism as the method of choice[4].

Finally, the equivalent circuit model is optimized and verified for accuracy by correcting its response to the physical response of the system. We implement an *Error Optimization* algorithm to both optimize the circuit parameters $C$, $R_L$, $R_T$ and $L_T$ and to

[4] The difference in the Fourier coefficients ascertains at a glance, the accuracy of the simulated current response with reference to its physical counterpart.

correct the simulated response, $I_{S,MOD}$, with the result that it closely matches the physical response $I_{S,MEAS}$. The *Error Optimization* algorithm minimizes the difference between the responses through an iterative feedback correction mechanism that involves varying the circuit parameters $C$, $R_L$, $R_T$ and $L_T$ sequentially. We vary the parameter most sensitive to error minimization during the iterations while the rest are held constant. *Load Response* of the rectifier circuit is then determined in accordance with the revised parameters values to generate the corrected simulated response, $I_{S,MOD}$, for that iteration. Next, the *Error Calculation* algorithm updates the difference between the revised simulated response, $I_{S,MOD}$, and the reference physical response $I_{S,MEAS}$. The process repeats with next most sensitive parameter varied and it continues up to the point at which the simulated response is able to replicate the physical response for a unique set of optimized circuit parameters.

Having successfully performed *Error Optimization* and having determined a unique *Correction Factor* for the equivalent circuit model, we are now able to theoretically predict the response $I_S$ of the system, for a harmonic supply-voltage including a pure 60 Hz sinusoidal voltage. The three algorithms we have described, *Load Response, Error Calculation* and *Error Optimization,* are collectively known as *Response Optimization algorithms.* They are implemented and executed in FORTRAN-90.

## 2. EXPLAINING THE EQUIVALENT CIRCUIT MODEL

### 2.1. Circuit Description

In Figure 4.2 we have illustrated an aggregate of N single-phase power-electronics loads, consolidated into an equivalent circuit model that applies to a single load connected to a harmonic voltage source via a shared transformer. The circuit shown in Figure 4.2 is an electrical equivalent of the circuit displayed in Figure 4.1.

The diode bridge rectifier circuit forms an interface, in the equivalent circuit model, between voltage supply and the resistive load connected at its output. The main parameters that define this equivalent circuit are:

- Discharging capacitance *C* of the rectifier circuit,
- Resistive load $P_L$ connected across the rectifier circuit. Load impedance is expressed as,

$$R_L = V_O^2 / P_L$$

- Consolidated system impedance, identified by a series combination consisting of Thevenin's equivalent impedance, shared-transformer impedance and the equivalent branch impedance of N parallel circuits connected to the point of common coupling. It is represented in terms of the system resistance $R_T$ and system inductance $L_T$. Mathematically,

$$Z_T = R_T + j\omega L_T$$

$$\text{And, } Z_T = Z_{TH} + Z_{TRAN} + Z_B$$

$$\text{In other words, } Z_T = (R_{TH} + R_{TRAN} + R_B) + j\omega(L_{TH} + L_{TRAN} + L_B)$$

$$\text{Therefore, } R_T = (R_{TH} + R_{TRAN} + R_B) \;\&\; L_T = (L_{TH} + L_{TRAN} + L_B)$$

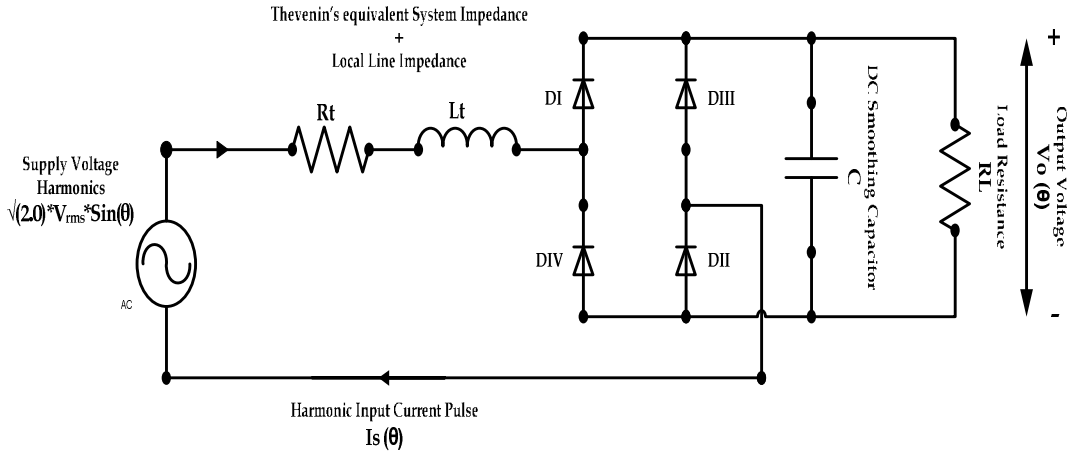



**Figure 4.2: Equivalent Circuit Model of Single-Phase Power Electronics load connected to an AC supply at the Point of Common Coupling.**

## 2.2. Circuit Operation

The diode bridge-rectifier circuit converts the 60 Hz AC voltage into a rectified DC signal measured across the resistive load. We can boradly classify the operation of a diode bridge rectifier circuit into two phases in one half-cycle of time period T = (1/60) sec, the *Charging Phase* and the *Discharging Phase*. These distinctions between, *Charging* and *Discharging* are based upon the behavior of the smoothing capacitor C in the two separate periods during one Time-cycle. Figure 4.3 illustrates the rectified voltage $V_O$ and input current pulse $I_S$ during the charging and the discharging phases of a diode bridge rectifier circuit.

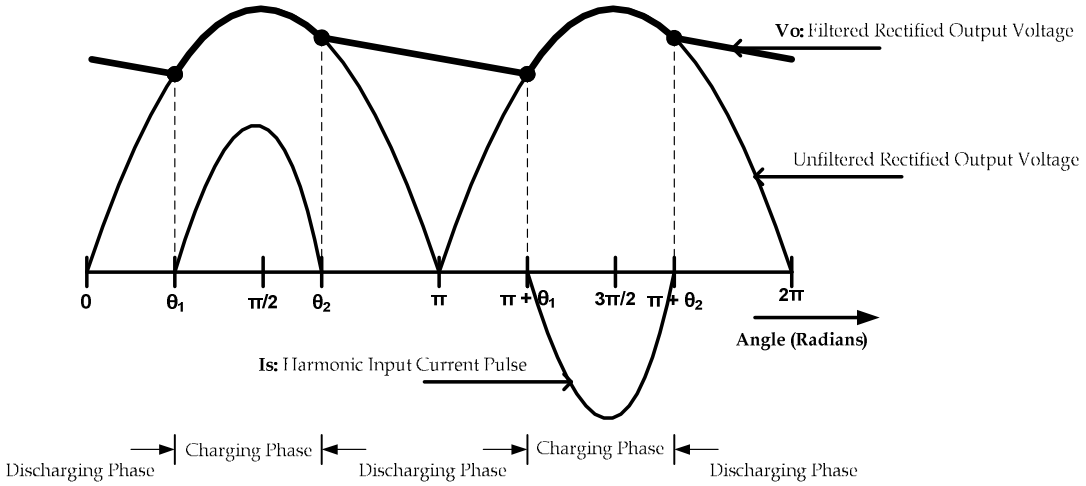



**Figure 4.3: Charging/ Discharging Phases of a Diode Bridge Rectifier Circuit**

*The Charging Phase*

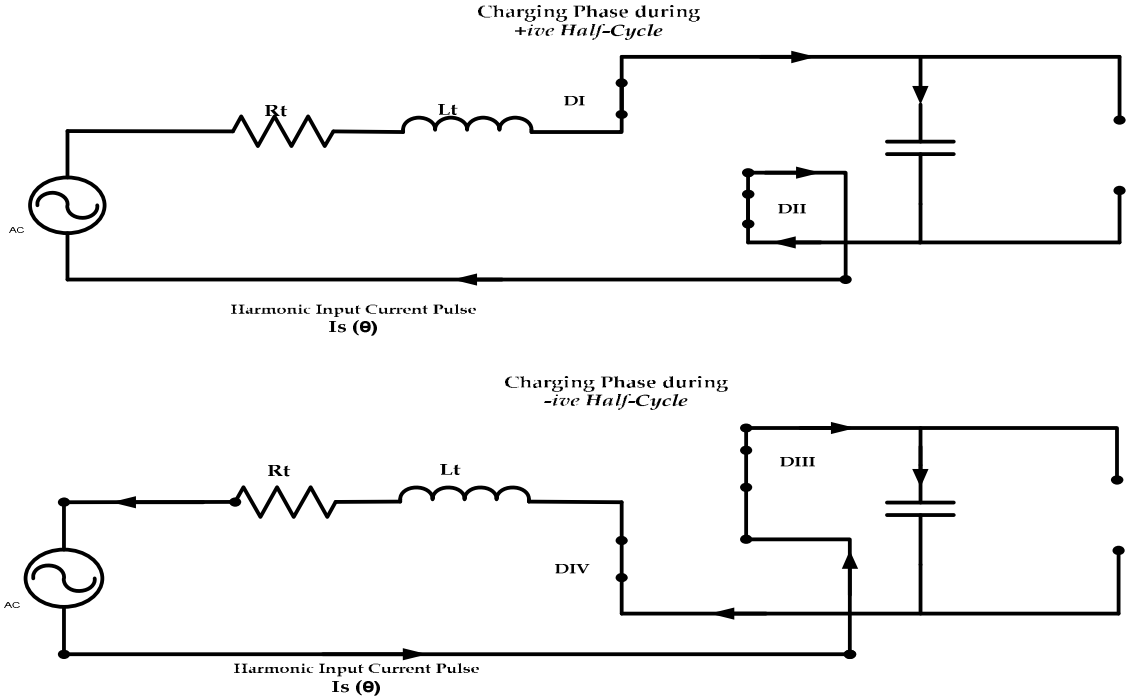



**Figure 4.4: Circuit Configuration of the DBR During the Charging Phase**

During the *Charging Phase*, an input current pulse, $I_S$, as shown in Figure 4.2, charges the DC smoothing capacitor C to the peak sinusoidal voltage value which is why

it is called the *"Charging Phase"*. Once the capacitor voltage equals the peak input sine voltage, the rectifier circuit stops charging the capacitor filter and the load current pulse $I_S$ falls to zero. The boundary equation that expresses this condition is expressed as:

$$I_S(\theta_2) = 0 \ldots BC1$$

At instant $t_2$, when the current pulse hits the zero value, we determine the corresponding angle $\theta_2 = \omega \times t_2$ degrees and $\omega = 2 \times \pi \times f$ radians/sec, where ω is the angular frequency and $f$ is the linear frequency 60 Hz. Hence, $\theta_2$ is the angle at which the current pulse crosses and falls below zero; it marks the end of the charging phase and beginning of the *Discharging* phase.

*The Discharging Phase*

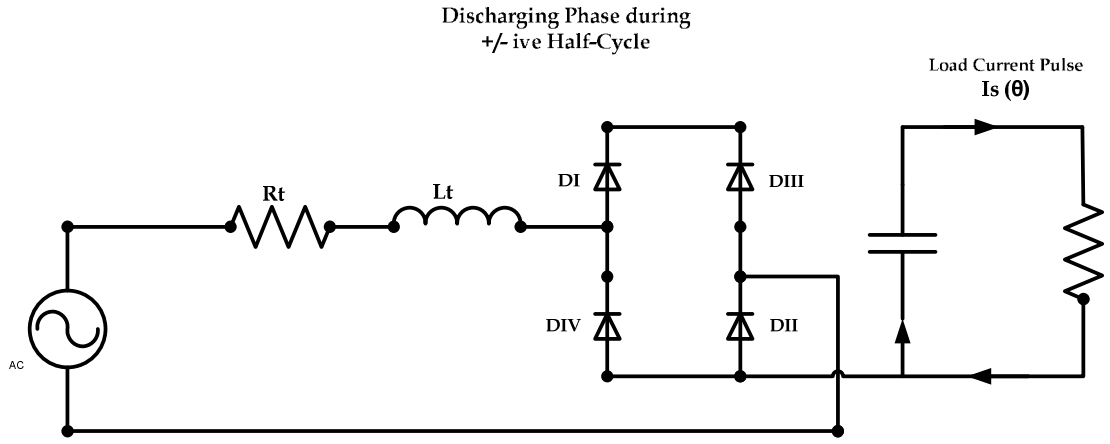



**Figure 4.5: Circuit Configuration of the DBR During the Discharging Phase**

The capacitor filter discharges through the load with the load current $I_S$. The capacitor voltage reduces exponentially while the supply-voltage rises again in the negative half-cycle. At instant $t_1$, when the capacitor voltage falls below the input sine voltage, the process of *Discharging* ends, which corresponds to the angle $\theta_1 = \omega \times t_1$ describing that instant. This condition is expressed by the following boundary equation:

$$V_O(\theta_1) \times e^{(\theta_2-\theta_2-\pi)\times(R_{L/\omega})} = (\sqrt{2.0}) \times V_{PEAK} \times Sin(\theta_1) \ldots BC2$$

The process of charging and discharging repeats in the negative half-cycle; the capacitor filter charges once again to a maximum value of the peak sinusoidal input voltage. The current pulse generated during the negative half cycle is the inverse of the current pulse generated in the positive half cycle.

### 2.3. Mathematical Representation of the Circuit Response

The response of the equivalent circuit is expressed in terms of the input current pulse $I_S$. This current-pulse is rich in harmonics with a Total Harmonic Distortion (THDI) of the order of 100%, expressed as the ratio of the sinusoidal input voltage and the consolidated system impedance of equivalent circuit $Z_T = R_T + j\omega L_T$. [5]

This equivalent system impedance is a function of the distance between the load and the PCC. For a fixed input supply voltage, the greater the distance, the higher will be the branch impedance $Z_B$ and corresponding impedance $Z_T$; and the smaller will be the input current pulse $I_S$.

Other factors do influence the current pulse. Notably, load power $P_L$ will affect the shape of the current pulse. As the load power increases, the shape of the current pulse becomes taller, wider and more skewed to the right. The increase has other effects: In addition to the load power variation, there is an attenuation effect on the harmonic current magnitudes (expressed as a percent of the fundamental) and significant impact of the phase angles variation, especially on higher-order harmonics. If the magnitude reduction due to *attenuation* and the cancellation of harmonics due to *phase diversity* are ignored, the harmonic content of the input current pulse may easily be overestimated. This over-

[5] Throughout the study we assume that the semiconductor diodes of the bridge-rectifier circuit are ordinary switches while the load connected to the rectifier circuit is resistive. Hence, the harmonic distortion in the input current pulse is not attributable to either of these devices.

estimation is not that critical when we are dealing with merely a few loads connected at the PCC, but as those harmonics producing loads proliferate, the overestimation may prove to a critical error. Similar variations occur with changes in the system impedance magnitude and X/R ratio. While variation in discharging capacitance *C* has a minor effect on current pulse, the variations of all these parameters collectively can significantly impact the harmonic content of the input current pulse $I_S$.

As we have already observed, the mathematical model of the capacitor-filtered diode bridge-rectifier circuit is expressed in terms of the analytical expression for the load current $I_S$ and the rectified output voltage $V_O$. The response of the circuit model, however, is expressed solely in terms of the input current pulse. Both expressions for $I_S$ and $V_O$ are functions of the input supply voltage $V_{IN}$ and the circuit parameters - discharging capacitance *C*,the resistive load $R_L$ and the collective system impedance $Z_T = R_T + j\omega L_T$ of a capacitor-filtered diode-bridge rectifier circuit.

The harmonic input voltage is written as,

$$V_{IN}(\theta) = \sqrt{2.0}\sum_N E(n) \times Sin(n\theta + \emptyset(n) + n\theta_1) \ldots (1)$$

Where N = an odd harmonic number from 1 through 25

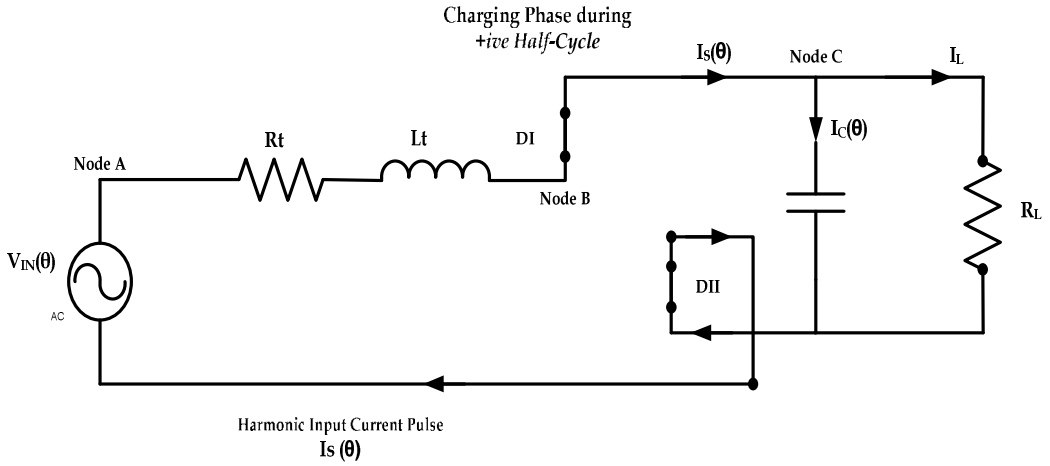



**Figure 4.6: Circuit Operation During the Charging Phase**

Figure 4.6 depicts the flow of the current pulse during the charging phase of the positive half-cycle[6]. Upon applying KCL at Node C, we observe the following relationship,

$$I_S(\theta) = I_C(\theta) + I_L(\theta)$$

This equation can also be expressed as,

$$I_S(\theta) = \omega C \frac{dV_O(\theta)}{d\theta} + \frac{V_O(\theta)}{R_L} \quad \ldots (2)$$

Similarly, KVL applied to the entire circuit reveals the following voltage equation,

$$V_{IN}(\theta) = I_S(\theta) \times R_T + \omega L \frac{dI_S(\theta)}{d\theta} + V_O(\theta) \ldots (3)$$

Solving for $I_S(\theta)$ and $V_O(\theta)$ using equations (2) and (3) and the boundary conditions represented in equations BC1 and BC2, we derive the following expressions,

$$I_S(\theta) = f(E(n), n, \theta, C, R_L, R_T, L_T) \ldots (4)$$

$$\text{And } V_O(\theta) = f(E(n), n, \theta, C, R_L, R_T, L_T) \ldots (5)$$

[6] The flow of the current $I_S$ during the charging phases in both the negative and positive half cycles allows the capacitor *C* to maintain its voltage polarity. The load current always flows in the same direction.

Equation (4) is the mathematical expression for the response of the equivalent circuit model for N single-phase bridge-rectified power electronics loads connected at a common distribution network via common shared transformer. Since $I_S(\theta)$ and $V_O(\theta)$ are time-varying signals, they are expressed as a function of the angle $\theta = \omega \times t$, where, $\omega$ is the angular frequency = $2\pi f$, and f is the linear frequency = 60 Hz. Derivation of this mathematical expression is detailed in Appendix A.

## 3. CONSTRUCTING *RESPONSE OPTIMIZATION* ALGORITHMS

Successful implementation of an analytical model is contingent upon its successful design, and the accuracy of its response. Section 2 explained the design and creation of our circuit model; we now move on to the verification of the accuracy of our equivalent circuit model, which occurs in three steps,

1. Response Generation – The first step involves generating the response of the equivalent circuit model. A *Load Response* algorithm is developed to determine the response of the circuit for a sinusoidal input voltage with an already known harmonic content. It is based on the analytical model (as described in Section 2) of the equivalent circuit.
2. Response Comparison – Once the response of the circuitis, determined, it is then compared to the actual physical response of the circuit, using an *Error Calculation* algorithm. As mentioned before, the response of the equivalent circuit model is measured in terms of the input charging current pulse $I_S$.
3. Response Optimization – The response of the analytical model is corrected iteratively and optimized through a feedback correction mechanism until it replicates the physical response. We will employ an *Error Optimization* algorithm

to minimize the differences between the two current pulses $I_{S,MEAS}$ and $I_{S,MOD}$ for a unique solution of the circuit parameters that define the equivalent circuit.

The three algorithms are written and compiled in FORTRAN – 90, and we explain each in detail in the subsequent sections:

### 3.1. Response Generation – *Load Response*

The load response algorithm is used to determine the input charging current pulse generated for an equivalent circuit model, powered by a harmonic sinusoidal voltage source, during the model's charging phase. For a given set of circuit parameter values $C$, $R_L$, $R_T$ and $L_T$ and the harmonic input voltage $Vin(\theta)$, the load response algorithm will determine the input current pulse $I_S(\theta)$ and the rectified output voltage $Vo(\theta)$ values for a time-period, T = 1/60 Hz. The input current pulse, however, is the designated simulated response, and it is to the generation of this alone that we will limit our discussion.

#### *3.1.1. Algorithm Logic –*

We use the Gauss-Seidel approach to implement the algorithm needed to determine the load response. The following sequence of steps is employed for the algorithm.

1. For an initial estimate $\theta_1$, using boundary condition BC1, solve for angle $\theta_2$, where the load current pulse $I_S(\theta_2)$ crosses the zero axis between 90 and 180-degrees.
2. Substitute the value of $\theta_2$ in boundary condition BC2 and solve for angle $\theta_1$.
3. For the updated values of $\theta_1$ and $\theta_2$, repeat steps (1) and (2) till the boundary conditions are satisfied within a specified tolerance. In this algorithm, the tolerance set for the load current pulse, $I_S(\theta_1)$ *at* $\theta_2$, for boundary condition BC1 is

0.5 Amps. The tolerance set for the rectified output voltage, $V_O(\theta)$ *at* $\theta_1$, for boundary condition BC2 is 0.03 Volts.

4. The value of $I_S(\theta)$ during the *Discharging* phase is maintained at zero amperes.

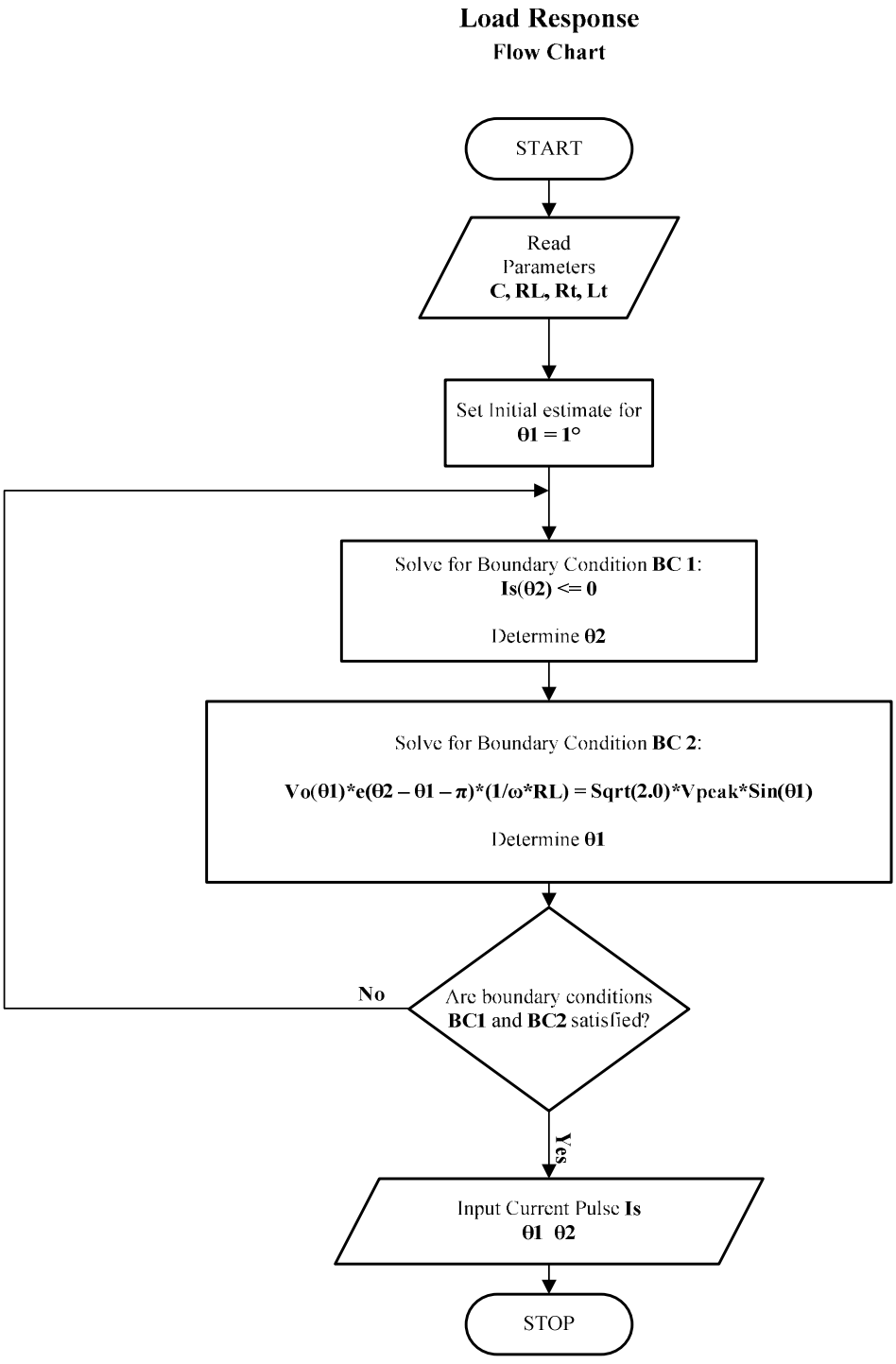



**Figure 4.7: Flow Chart for Load Response**

*3.1.2. A Case Study*

An equivalent circuit model powered by 120 Vrms AC source is connected to a 100 MW load with the following parameter values as listed in Table 4.1:

| $P_L$ (MW) | C (μF) | $R_L$ (Ω) | $R_T$ (Ω) | $L_T$ (mH) |
|---|---|---|---|---|
| 100 | 224.79 | 871 | 2.73 | 0.81 |

**Table 4.1: Circuit Parameter Values of an Equivalent Circuit Model**

Execution of the *Load Response* algorithm generates the following response for the given circuit model:

| $I_{S,MEAS,\ PEAK}$ (A) | $\theta_1$ (Deg) | $\theta_2$ (Deg) |
|---|---|---|
| 1.94 | 74.08 | 104.81 |

**Table 4.2: Load Response of the Equivalent Circuit Model**

The load response for the given circuit is illustrated below in Figure 4.8:

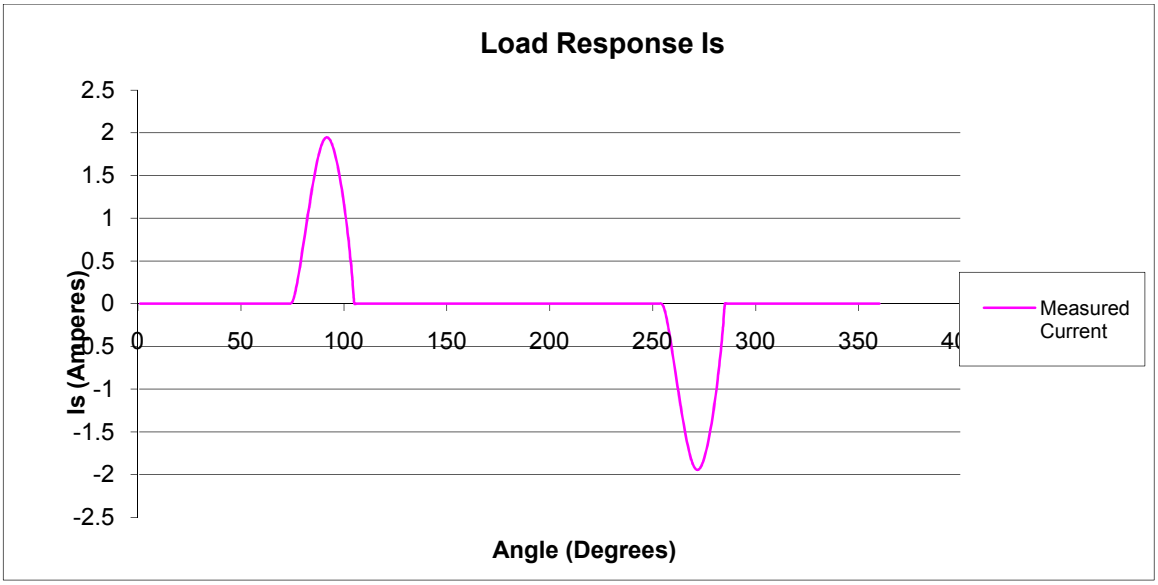



**Figure 4.8: Load Response for an Equivalent Circuit Model**

### 3.2. Response Comparison – *Error Calculation*

The *Error Calculation* algorithm determines the difference between the desired (reference) current $I_{S,MEAS}$ and the simulated load current $I_{S,MOD}$. This difference can be determined as the sum of the differences between the values of two current pulses, calculated at each degree for a 360-degrees cycle. This sum of differences represents the inverse of the extent of the optimization of the simulated current response as it emulating the actual physical response.

Differences in the harmonic coefficients of the two current pulses can also used to measure the correction in $I_{S,MEAS}$.

*3.2.1. Algorithm Logic –*

*The following is the sequence by which the Error Calculation* algorithm isimplemented.

1. The *Load Response,* $Is_{meas}$ is calculated and stored as an array of 360 data points corresponding to a 360-degrees cycle. The reference load response, $I_{S,MOD}$ is stored as an array of the same length.

```
Do i = 1, 180, 1

  Ei_total_2 = Ei_total_2 + ABS(Id(i) - Ia(i))
  Ev_total = Ev_total +  ABS(Vd(i) - Va(i))

End Do
```

**Figure 4.9: Illustration of the Error Calculation Subroutine**

2. The absolute difference between $I_{S,MEAS}$ and $I_{S,MOD}$ is determined at each degree for a 180-degrees half-cycle (as illustrated in Figure 4.4). The sum of the 360 error data points is calculated as twice that of the 180-degrees half-cycle. This consolidated error represents the difference between the simulated and the physical response of the equivalent circuit. It is labeled as *Ei*.

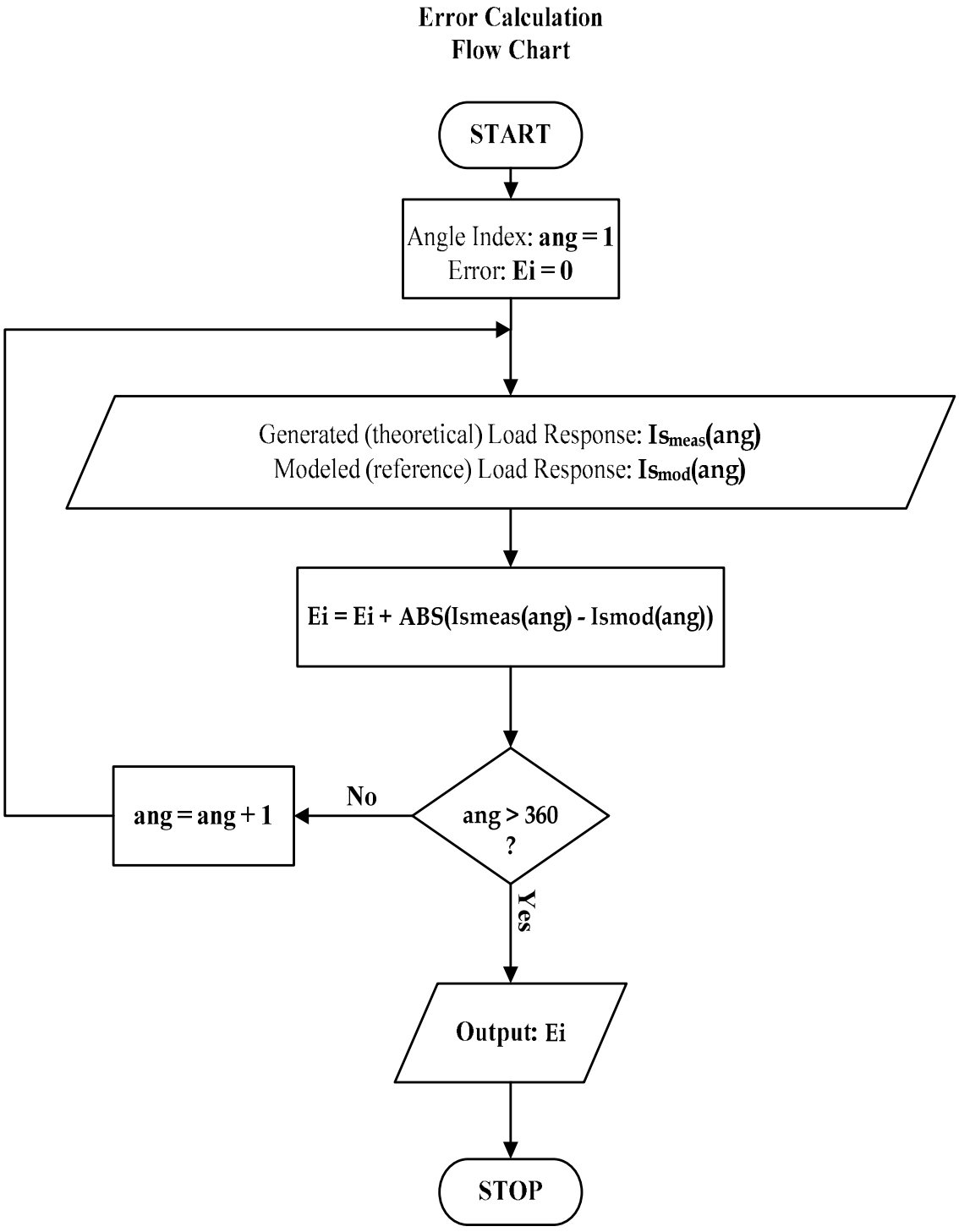



**Figure 4.10: Flow Chart for Error Calculation**

*3.2.2. A Case Study*

We connect an equivalent circuit powered by 120 Vrms AC source to a 100 MW load with the following parameter values, as listed in Table 4.3:

| $P_L$ (MW) | C (μF) | $R_L$ (Ω) | $R_T$ (Ω) | $L_T$ (mH) |
|---|---|---|---|---|
| 100 | 1110.03 | 144.13 | 4.41 | 5.85 |

**Table 4.3: Circuit Parameter Values of an Equivalent Circuit Model**

Execution of the *Load Response* algorithm generates the following response for the given circuit model, as illustrated in Table 4.4:

| $I_{S,MEAS,\ PEAK}$ (A) | $\theta_1$ (Deg) | $\theta_2$ (Deg) |
|---|---|---|
| 4.30 | 60.31 | 134.62 |

**Table 4.4: Load Response of the Equivalent Circuit Model**

The load response for both the given circuit and the actual physical response are illustrated in Figure 4.11:

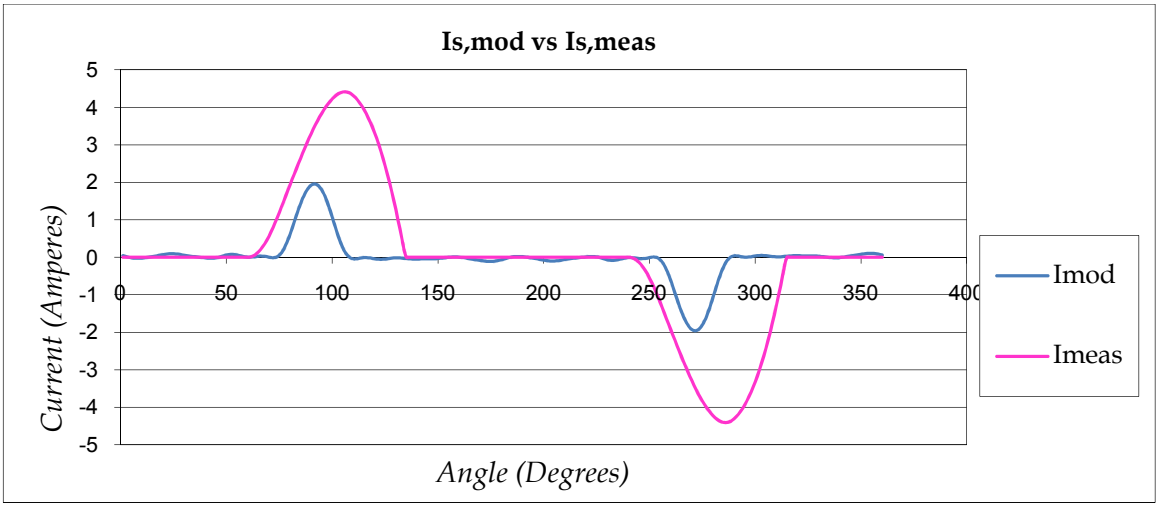



**Figure 4.11: Response Comparison for an Equivalent Circuit Model**

The consolidated difference between the two current responses, *Ei* = 556.07 A. . . *(6)*

### 3.3. Response Optimization – *Error Optimization*

By *Response optimization*, we are referring to the process of optimizing the parameters of a capacitor-filtered diode-bridge rectifier circuit through its analytical model, which is achieved when the generated load response, $I_{S,MOD}$ matches a reference load response, $I_{S,MEAS}$ for a given supply voltage input.

We optimize the parameters iteratively, based on their ability to decrease the difference between the load response simulated by the analytical model and the actual load response of the circuit, for the same supply-voltage input.

We first vary the most sensitive parameter, holding the remaining parameters constant; then we use the updated combination of the parameters to generate the load

current pulse by using the *Load Response* algorithm. At this point we revise the difference between $I_{S,MEAS}$ and $I_{S,MOD}$ by using the *Error Calculation* algorithm for that iteration. Once a parameter is modified, we don't consider it for further optimization until the remaining parameters have been optimized once for that iteration. Once all the parameters have been updated, we simply repeat the cycle of optimization until each parameter has been modified to its optimum value.

This process can be viewed as constructing the shortest path to achieve the optimized response of the capacitor-filtered diode-bridge rectifier circuit as each time we alter the most sensitive parameter, it results in maximum optimization.

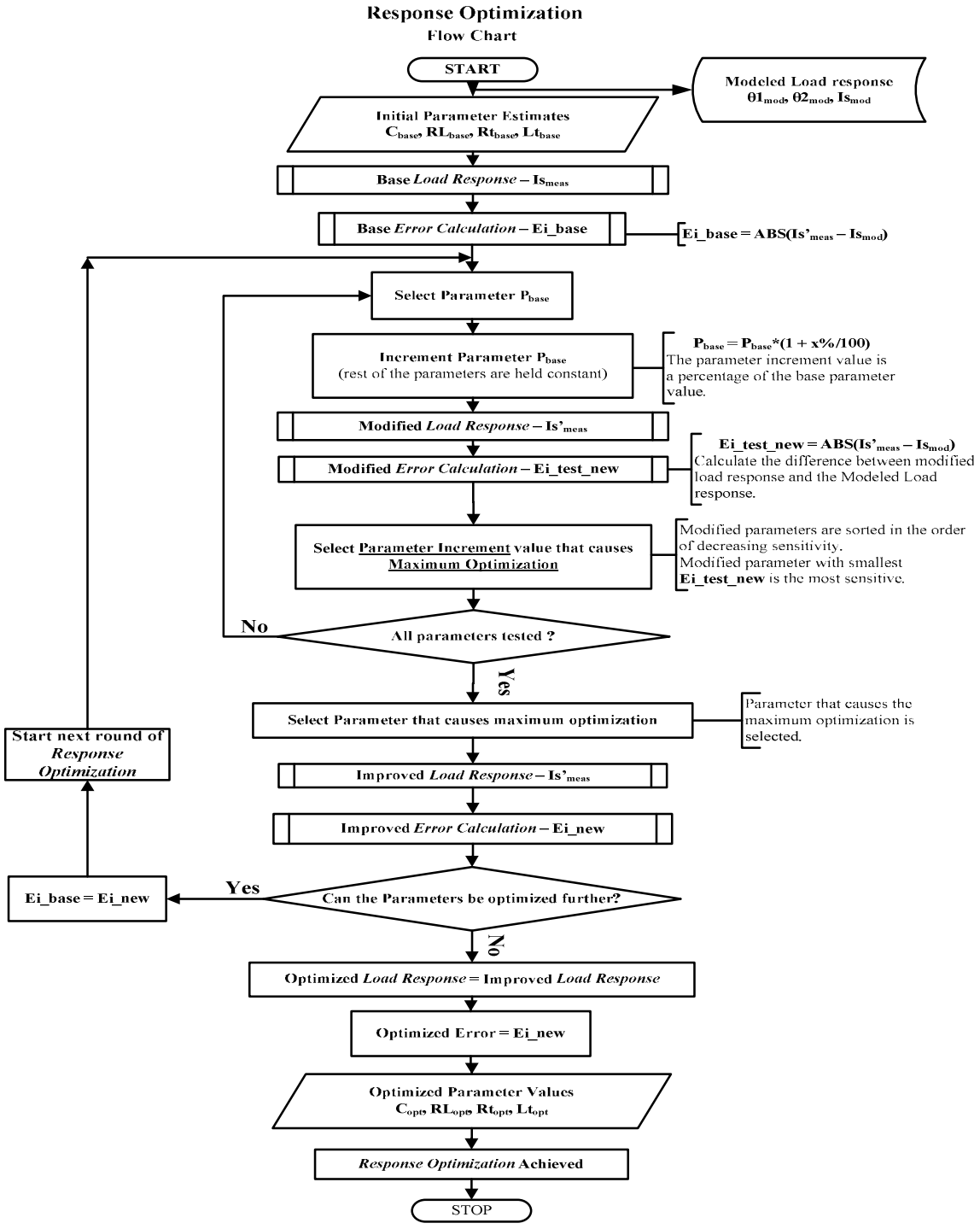



**Figure 4.12: Flow Chart for Error Optimization**

*3.3.1. Algorithm Logic –*

The algorithm for *Error Optimization* is executed through finite-differences. We use the following sequence of steps in order to implement the algorithm:

1. We make an initial estimation of the parameters necessary to begin the process of optimization. This estimation of parameters is determined using the following equations:

$$C_{Discharging}(\mu F) = 2 \times T_{Off} \times \frac{P_L}{(1-0.9^2)} \times \left(V_{in,fundamental}^2\right) \ldots (7)$$

$$R_L\,(\Omega) = \frac{V_{in,fundamental}^2}{P_L} \ldots (8)$$

$$R_T(\Omega) = V_{in,fundamental} \times \frac{(1-0.98)}{I_{des,rms}} \ldots (9)$$

$$L_T(mH) = \left(\frac{X}{R}\right) \times \frac{R_t}{(120 \times PI)} \ldots (10)$$

$$T_{Off}(sec) = \frac{\left(2 \times PI + (\theta_{1,des} - \theta_{2,des})\right)}{120 \times PI} \ldots (11)$$

Where,

$T_{Off}$ – Duration of the *Discharging* phase in seconds.

$\theta_{1,des}$ – Angle in degrees when the *Charging* phase begins

$\theta_{2,des}$ – Angle in degrees when the *Discharging* phase begins

$Where-$ 0.98 is based on the assumption that $V_{OUT}$ = 98% of $V_{IN}$ and

$V_T = V_{IN} - V_{OUT}$

This initial estimate of the parameters is collectively referred to as the base parameter value.

2. Each parameter is limited to within a range. A given parameter *P* varies between an upper-limit *U = P*1000* and a lower-limit of *L = P/1000*. Once we have calculated the parameter ranges, these boundary values will remain unchanged through the course of *Error Optimization* algorithm.
3. *Load Response* for each parameter variation is determined in terms of the harmonic load current pulse, $I_{S,MEAS}$

4. We calculate the difference between the generated load current pulse, $I_{S,MOD}$, and reference current pulse $I_{S,MEAS}$, using the *Error Calculation* algorithm. This difference is referred to as the base difference *Ei_base*. *Ei_base* is the sum of the differences between the absolute values of $I_{S,MOD}$ and $I_{S,MEAS}$ at each degree across a complete 360-degrees cycle.

$$Ei_{BASE} = \sum_{ANG\,=\,1}^{360} ABS\big(I_{S,MOD}(ang) - I_{S,MEAS}(ang)\big) \ldots (12)$$

We vary only one parameter during iteration, while holding the others constant. The change in the base parameter value is referred to as *Parameter Increment and* is calculated as a percentage of the lower-limit of a parameter.

$$Param\_Incr = L \times \frac{Pcent}{100} \ldots (13)$$

Where,

*Param_Incr – Parameter Increment* value added to the base parameter *P*

*Pcent* – Percentage is used to calculate the *Param_Incr.*

*L* – Lower-limit of parameter *P*

```
Subroutine Parameter_increment(pcent, Del, L)
    !Declaration

        Real, INTENT(OUT)::Del
        Real, INTENT(IN):: L
        Real,INTENT(IN):: pcent
    ! Initialization

      Del = 0.0

    ! Execution

      Print*, "Pecentage you've entered", pcent
      Del = L*pcent/100

      Print*,""
      Print*, "Parameter Increment now equals:", Del
End Subroutine Parameter_increment
```

**Figure 4.13: Illustration of the Parameter Increment Subroutine**

5. For a given parameter *P*, we calculate a set of parameter increment values for a set of percentages (as is shown in equation 13). The base value is then increased (or decreased) for all *Parameter Increment* values as shown in equations (14) and (15).

$$P^1_{base} + Param\_Incr_1 = P^1_1 \ldots (14)$$

$$P^1_{base} + Param\_Incr_2 = P^1_2 \ldots (15)$$

6. *Each parameter's Load Response* is determined when incremented by the *Parameter Increment* value that it is assigned (while the rest of the parameters are held constant).

$$(P^1_1, P^2_{base}, P^3_{base}, P^4_{base}) \rightarrow Load\ Response \rightarrow I^1_{S1,MOD} \ldots (18)$$

$$(P^1_2, P^2_{base}, P^3_{base}, P^4_{base}) \rightarrow Load\ Response \rightarrow I^1_{S2,MOD} \ldots (19)$$

7. Of those responses, the *Parameter Increment* value that causes maximum error correction is considered as "the *Parameter Increment* of choice", selected to optimize that parameter. This process is then repeated for each parameter.

$$(I^1_{s1,MOD}, I_{s,MOD}) \rightarrow Error\ Calculation \rightarrow Error_1 \ldots (20)$$

$$(I^2_{s1,MOD}, I_{s,MEAS}) \rightarrow Error\ Calculation \rightarrow Error_2 \ldots (21)$$

If, $Error_1 < Error_2$

Then, $Param\_Incr_1$ is chosen to increment parameter $P^1_{base}$

8. We sort the *Load Response*s for all parameters values in the order of decreasing sensitivity to the correction caused by each parameter variation, between the generated load current pulse $I_{S,MOD}$ and the reference load current pulse $I_{S,MEAS}$. In other words, the order of decreasing error calculated between $I_{S,MOD}$ and $I_{S,MEAS}$ determines the sorting of the parameters and their load responses.
9. We revise the parameter variation that causes the maximum correction to its incremented value. We then determine the *Load Response*. Finally, the *Error Calculation* algorithm is employed to calculate the new sum of differences between the theoretical and the modeled load current pulse. This sum is labeled as *Ei_new*.
10. *Ei_new* replaces the old value stored in *Ei_base* or in other words, *Ei_new* is the new *Ei_base.* The revised parameter value, together with the other parameter values held constant for this iteration are now referred to as the new base parameter values.
11. Once a given parameter is varied, it is not considered for further revision during the next round of optimization. Rather, it is held constant at its current revised value till all the remaining parameters have been optimized. We must do this in order to ensure that the optimization of the set of parameters is balanced, and also to prevent the skewing of the *Error Optimization* process by the uneven variation of the parameters.
12. The process repeats itself to optimize the remaining parameters.
13. We call the cycle of optimization complete when we have optimized all parameters once for that cycle.

14. This process iterates until we cannot reduce the difference between the theoretical, $I_{S,MOD}$ and the reference $I_{S,MEAS}$ current pulse any further.

The process of *Error Optimization* concludes at this point. We now have an optimized set of circuit parameters, also called the *Correction Factor* that yields a theoretical input current pulse $I_{S,\,MOD}$ with an accurate harmonic content, as predicted.

*3.3.2. A Case Study*

Taking our initial estimate of parameters in Section 3.2.1, which yielded an error *Ei_Base = 556.07 A (eqn. 8)*, we can now analyze our case study. For an initial estimate of the parameter values listed in Table 4.3, the corresponding load response of the equivalent circuit is given in Figure 4.11. This initial response of the given equivalent circuit is optimized in this section.

The simulated response is corrected to a unique optimized *Correction Factor*, so that it closely matches the actual response of the circuit. We will minimize the difference between the corrected current pulse and the reference current pulse in this case to *Ei_new = 19.64 A.* The final solution of the parameter values is listed in Table 4.5

| Parameters | $P_L$ (MW) | Ei (A) | C (µF) | $R_L$ (Ω) | $R_T$ (Ω) | $L_T$ (mH) |
|---|---|---|---|---|---|---|
| *Initial Estimate* | 100 | 556.87 | 1110.03 | 144.13 | 4.41 | 5.85 |
| *Final Solution* | 100 | 19.64 | 224.79 | 871 | 2.73 | 0.81 |

**Table 4.5: Initial Estimate and Final Solution of Circuit Parameter Values for an Equivalent Circuit Model**

The execution of the *Load Response* algorithm generates the response we see in Table 4.6 for the optimized circuit model in comparison to the reference physical response.

| Circuit Response | $I_{S,MOD,\,PEAK}$ (A) | $\theta_1$ (Deg) | $\theta_2$ (Deg) |
|---|---|---|---|
| *Physical* | 1.96 | 73.2 | 104.9 |
| *Optimized* | 1.94 | 74.079 | 104.81 |
| *ABS (Difference)* | 0.02 | 0.879 | 0.11 |

**Table 4.6: Load Response of the Equivalent Circuit Model**

The optimized load response for the given circuit and the actual physical response are illustrated together in Figure 4.14:

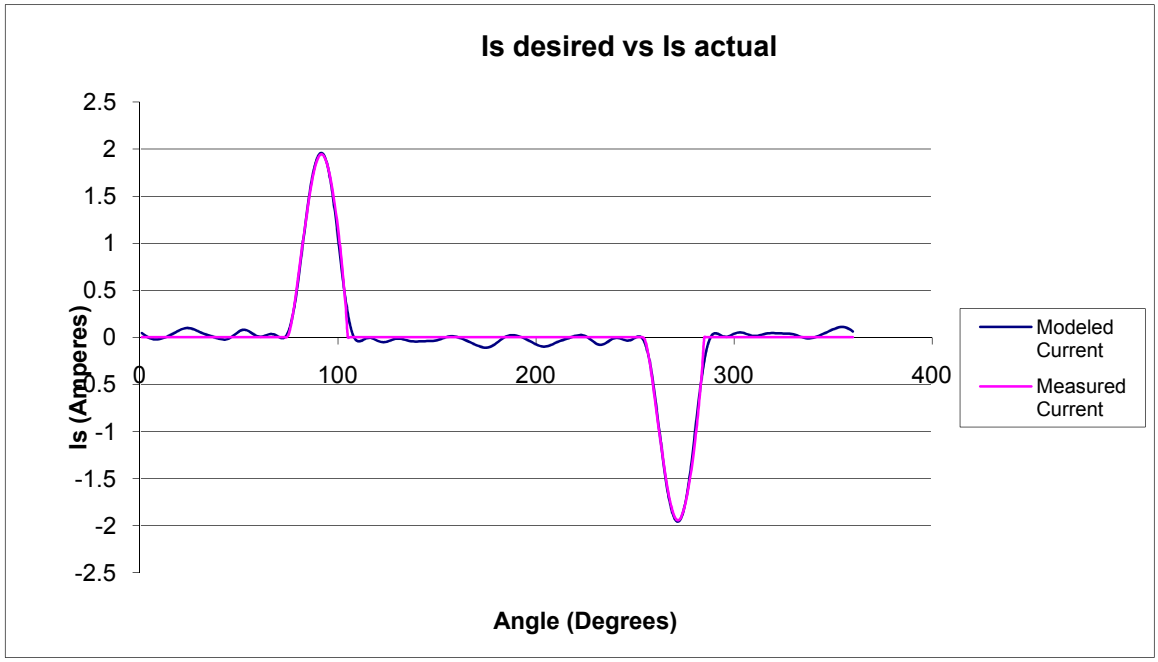



**Figure 4.14: Optimized Response of an Equivalent Circuit Model**

Comparison between the optimized load response and the physical load response is illustrated in Figure 4.15:

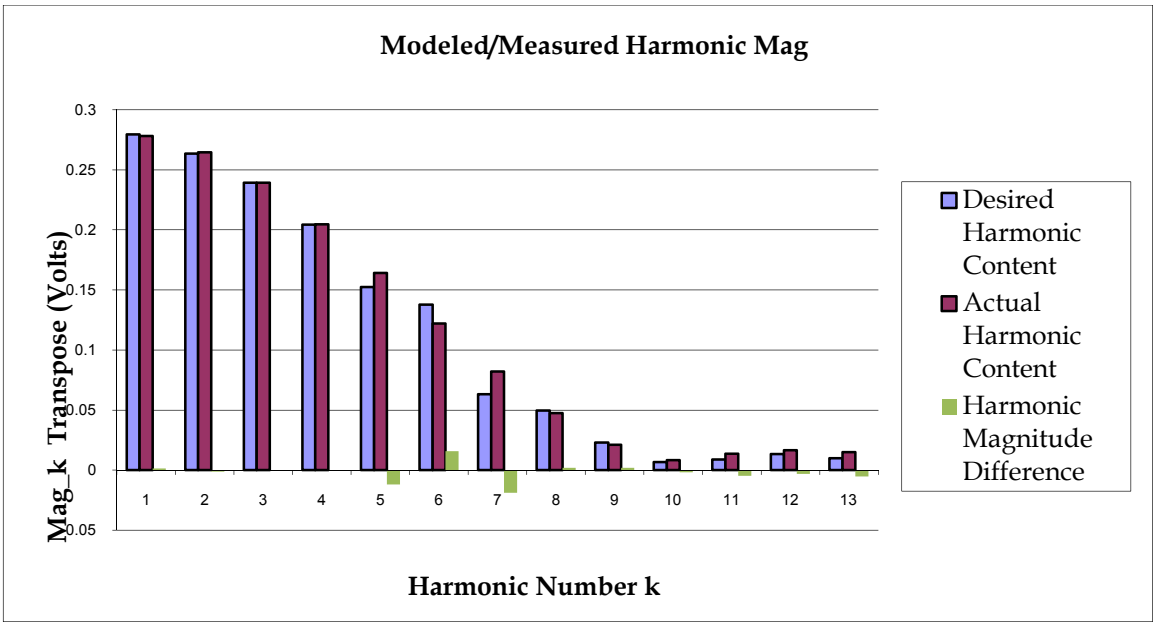



**Figure 4.15: Comparison of Harmonic Coefficients of the Optimized Modeled response versus the Physical Response**

## *4.* APPLICATION OF THE *RESPONSE OPTIMIZATION ALGORITHMS*

Let's consider the scenario illustrated in Figure 4.1 again – N parallel single-phase power electronics loads are connected to the point of common coupling through a shared,

non-linear Transformer, non-linear system impedance and individual non-linear branch impedances. The supply side of the distribution feeder network is connected to a harmonic voltage source. The existing power electronics loads contribute to the harmonic content of $I_L$, the supply current pulse that subsequently affects $I_{S,N}$, individual branch current, for a given load N. Additional harmonic loads proliferate within the distribution feeder network further exacerbating the harmonic content of the current supply.

Next, we power an equivalent circuit model representing N single-phase power electronics loads (as depicted in Figure 4.1) connected at the PCC and powered by the same harmonic supply voltage.

The *Response Optimization algorithms* are at the core of the optimization process. After defining initial estimates of the parameters, $C$, $R_L$, $R_T$ and $L_T$ we generate an initial response of the circuit is generated in terms of the input current pulse $I_{S,\ MEAS}$. Then we compare and correct this current pulse by applying our *Response Optimization* algorithms, in order to replicate, $I_{S,\ MEAS}$, our reference current pulse while optimizing the circuit parameters to a *Correction Factor*. This premits us to accurately model the equivalent current pulse with a unique solution of circuit parameters, also called the *Correction Factor*, so that the circuit response will match the actual current pulse, $I_{S,\ MEAS}$, for a given harmonic supply voltage. Once modeled, the equivalent circuit has the ability to theoretically predict, $I_{S,\ MOD}$, the current response of N single-phase power electronics loads, it emulates for a given voltage supply input at the point of common coupling.

In another scenario, to ensure that the current pulse generated by the equivalent circuit is restrained within acceptable harmonic limits, we optimize the response of the equivalent circuit model, $I_{L,\ MOD}$, to match the appropriate reference response. After we have calculated the *Correction Factor*, we still generate an optimized response of the equivalent circuit model for that particular harmonic supply voltage. The description of the *Correction Factor* depends on variations in the supply voltage, variations in X/R ratios, phase-shift variations, and the nature and number of loads connected to the distribution feeder network.

Subsequently, this optimized current signal is amplified, and fed to the actual load network through the Point of common coupling. A continuous real-time iterative process is, thus, established, which ensures that the actual supply current is optimized to a desired harmonic content before being injected into the point of common coupling.

Successful compliance testing depends upon determining, a *Correction Factor*, such that the equivalent circuit model generates a current pulse for a pure 60 Hz Sine wave supply.

# CHAPTER 5

# Harmonics Testing Station

## 1. INTRODUCTION

The Harmonics Testing Station is a LabView based experimental set-up, designed to examine the voltage conditions and conduct harmonic mitigation analysis at the point of common coupling (PCC) of a distribution feeder network. It conducts a correction mechanism to alleviate the harmonic content of the voltage at the PCC, referred to as *Load V*, and matches it to a reference voltage signal, *Target V,* with a known harmonic content.

The Testing Station can also be viewed as an experimental equivalent of the proposed analytical model of single-phase power electronics loads connected to a distribution feeder network, and powered by a sinusoidal harmonic voltage source. We can usef it to verify the predicted theoretical response of the proposed mathematical model. The mdoel is consideted valid, if the analytical model, which is powered by a voltage supply with user-defined harmonic content, generates a theoretical response $I_S$ and a unique *Correction Factor* such that it is consistent with the response of multiple single-phase power electronics loads connected to the Testing Station.

The comparison of *Load V* against a desired voltage *Target V* is equivalent to a comparison made between $I_{S,MOD}$ the simulated current pulse (the ratio of *Load V* and system impedance), and the $I_{S,MEAS}$ (the ratio of *Target V* and system impedance).

Finally, we can use the Testing Station to demonstrate the effect of *attenuation* and *partial self-compensation*. To demonstrate this, we simulate harmonic conditions at the PCC, and this in turn will permit us to study the interdependence between the voltage distortion at the PCC, and the distortion in the main supply current.

## 2. PRINCIPLE OF OPERATION

The Testing Station generates a reference voltage signal *Target V;* it contains a user-defined (therefore controllable) harmonic content. Once *Target V* is created, we input it into a Pulse-Width Modulated (PWM) amplifier. The amplifier's typical amplification factor is expressed as a ratio of its output voltage to the input voltage,

$$Output\ Signal/Input\ Signal \sim 120\ V/5\ V \ldots (1)$$

Our target amplified signal output from the power amplifier can be accurately measured under no-load or open-loop conditions at the PCC. In other words, the reference supply voltage equals the voltage at the point of common coupling. Mathematically,

$$Target\ V = Load\ V \ldots (2)$$

Connecting a load to the PCC completes the circuit (as shown in Figure 5.1). This will prompt a load current to flow from the source, through the amplifier, and finally to the load, which sets up an interaction of the load current with non-linear load impedance. The latter distorts *Load V*, the voltage potential measured at the PCC, which we can also be view as a voltage gradient across the connected load. Mathematically, *Load V* is expressed as,

$$Load\ V = I_L \times R_L \ldots (3)$$

The product of the load current, $I_L$, and non-linear amplifier impedance develops a harmonic potential across the amplifier. Applying KVL in Figure 5.1, the difference between the reference voltage, *Target V,* and the voltage across the amplifier also equals the voltage across the load. Therefore, *Load V* is also represented as,

$$Load\ V = Target\ V - I_L \times Z_{Amplifier} \ldots (4)$$

Therefore, as demonstrated in Equation 4, the *Load V* in a closed loop configuration must deviate from the *Target V*. In other words, in a closed loop, the voltage at the PCC is no longer a true reproduction of the reference supply voltage, *Target V*.

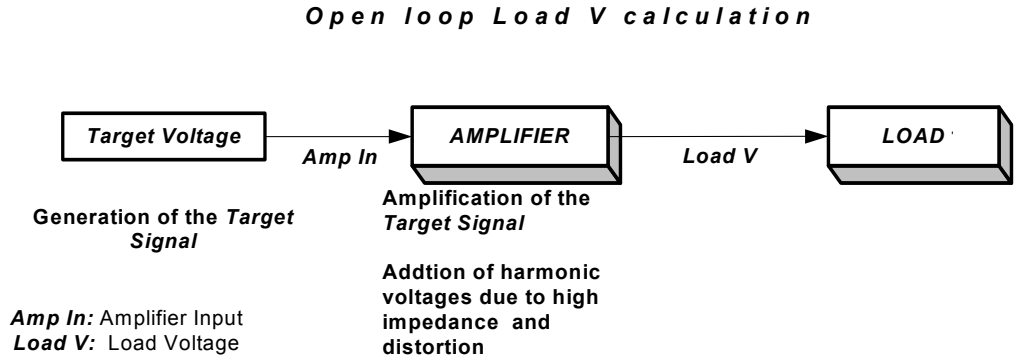



**Figure 5.1: Load V Distortion without Feedback**

### 2.1. Closed Loop Operation:

A closed loop operation deals with the process of correcting the signal, *Load V,* through a continuous *Manual Feedback operation*. Our objective to reduce the error between the *Target V* signal and the *Load V* signal manually, which can be accomplished by reducing the respective percentage magnitudes and adjusting the phases of the respective harmonics that are causing the error.

The closed-loop feedback operation is illustrated in the Figure 5.2. The *Testing Station* determines the error between the *Target V* signal and the *Load V* signal, and then adjusts the error through a manual feedback process of correction called *Manual Feedback Operation*[7]. The adjusted signal is output from the Testing station, and it is fed to the PWM amplifier. The amplifier generates the amplified *Load V* signal. This modified *Load V* signal is then input to the load, and it is fed back again into the Testing

[7] There are other methods of Error correction; these methods are discussed later in this chapter.

Station for the next iteration of feedback operation. Therefore, the process of creating a *Load V* signal as a faithful reproduction of *Target V* voltage, in terms of its harmonic content, magnitude, and phase is performed continuously and iteratively.

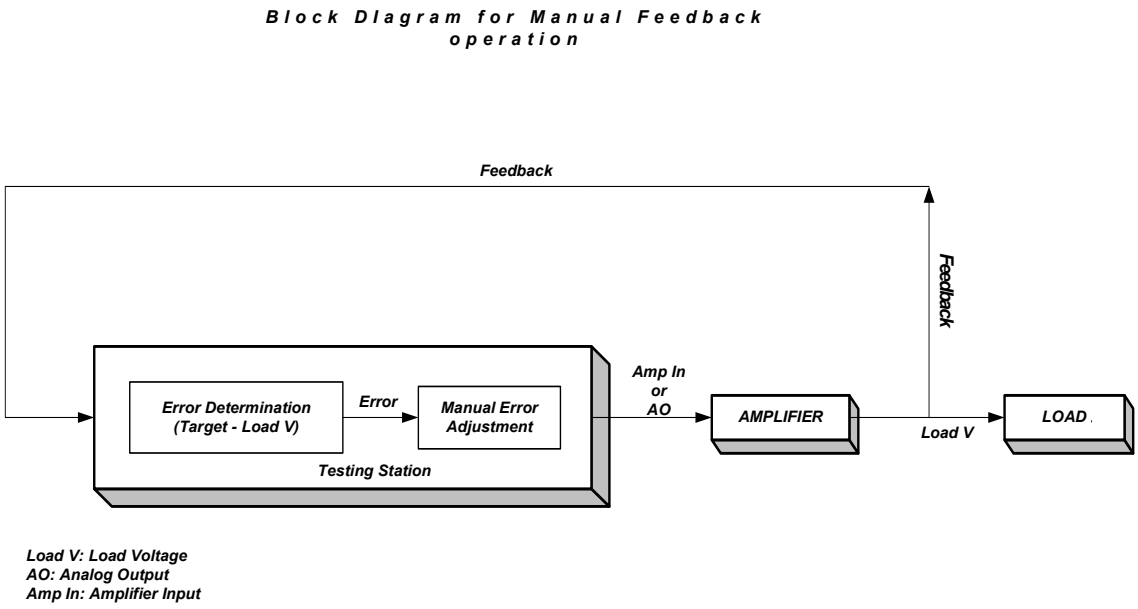



**Figure 5.2: Manual Feedback Operation**

The *Testing Station* has two modes of feedback operation:

- Summing Junction Mode
- Stand Alone Mode

### *2.1.1. Summing Junction Mode:*

In this mode, the difference between the *Target V Signal* and the *Load V* signal is computed. The computed error is manually adjusted through the *Manual Feedback Operation*. The error-adjusted signal is output from the *Testing Station* as the *AO* (Analog output) signal. It is input into the amplifier as the *Amp In* signal. The operation of a *Summing Junction Mode* is illustrated in Figure 5.3.

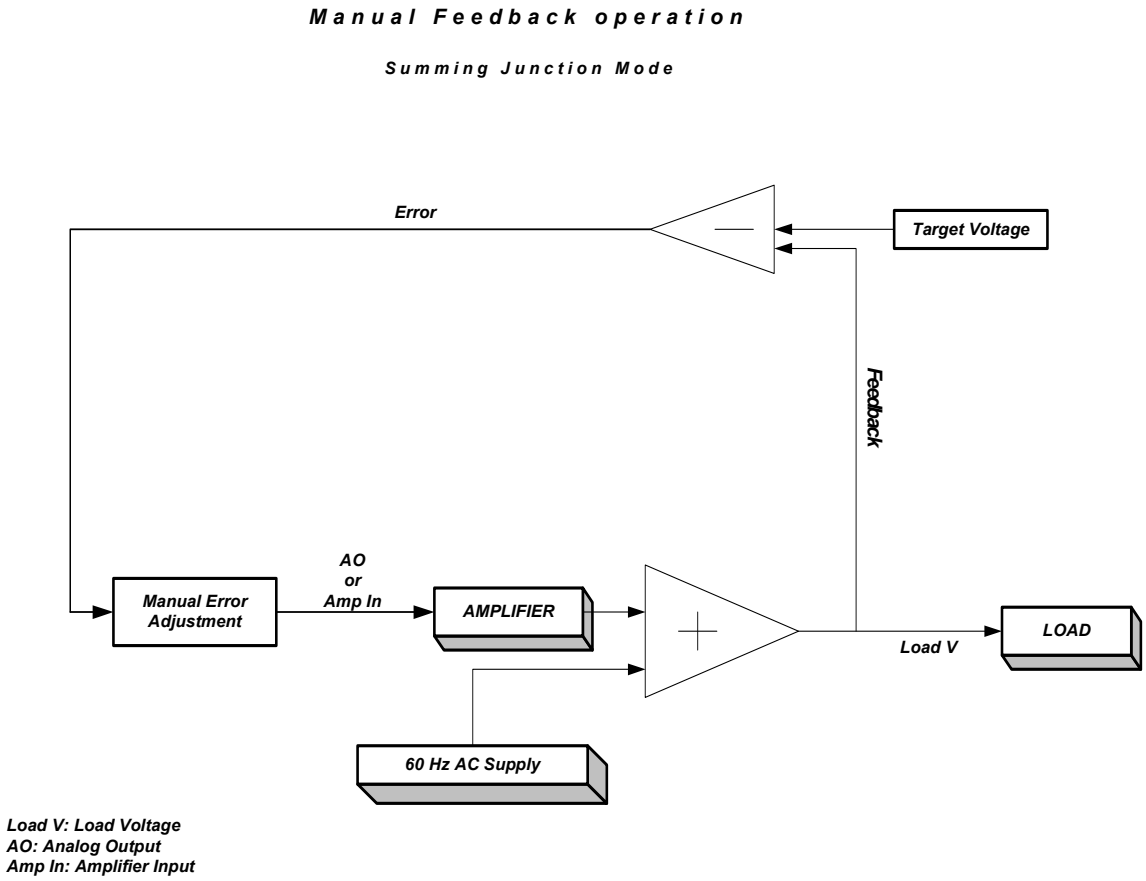



**Figure 5.3: Summing Junction Mode**

The amplifier output is added to the 60 Hz AC signal. The sum of the two signals constitutes the corrected *Load V* signal for the current feedback iteration. This *Load V* signal is fed to the load and fed back into the testing station to recalculate the harmonic difference between the *Target V* signal and the new *Load V* signal for the next iteration.

Thus in the given mode of operation, we can generate a new *Load V* signal with every iteration, through manual error adjustment of the difference between the *Target V* signal and the *Load V* signal (of the previous iteration), its amplification and its subsequent addition to the 60 Hz AC supply.

### *2.1.2. Stand Alone Mode:*

In this mode, the difference between the *Target V* signal and the *Load V* signal is calculated. We manually adjust the computed error through the *Manual Feedback Operation* method. The error-adjusted signal is then added to the *Target V* signal. The calculated signal is output from the *Testing Station* as the *AO* (Analog output) signal. It is input into the amplifier as the *Amp-In* signal. The signal processed in the amplifier is output as the *Load V* signal, which is fed to the load connected to the Testing Station, and it is also fed back to the *Testing Station* for the next feedback operation. The operation of a *Stand Alone Mode* is illustrated in Figure 5.4.

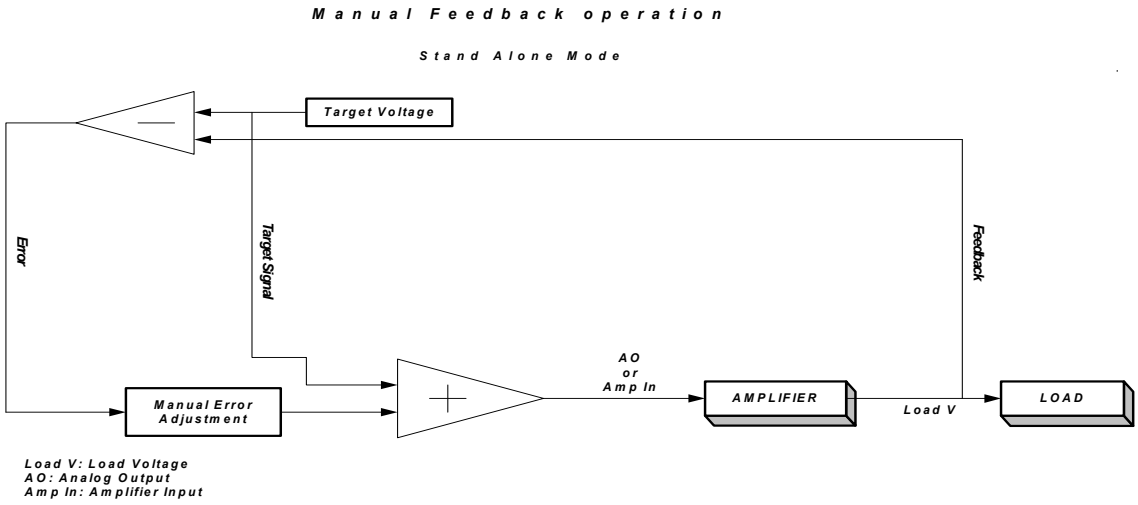



**Figure 5.4: Stand Alone Mode**

Thus, in the given mode, we add the error-adjusted signal to the *Target V* signal; their sum is input into the amplifier in order to generate the new *Load V* signal at the end of the current cycle, and beginning of the next one.

### *2.1.3. Stand Alone Mode v/s Summing Junction Mode*

In the *Stand Alone Mode,* the *Target V* signal is modified to generate the *Load V* signal by the addition of the error-adjusted signal and its subsequent amplification by an appropriate scale. Additionally, the Testing Station itself powers the signal with the addition of the *Target V* signal to the error-adjusted signal.

In the *Summing Junction Mode*, however, the error-adjusted signal is firstly amplified to the desired value and then added to a 60 Hz AC supply to construct the *Load V Signal*. The advantage of adding a 60 Hz is supply is that it provides for the 90% of the signal power.

The next section discusses the *Manual Feedback Operation* — the method used for correcting *Load V* to match the *Target V Signal*.

## 2.2. *Manual Feedback* Operation:

The *Manual Feedback* operation involves a way of nullifying the *"worst harmonic offender"* in the *Load V* signal, by manually changing the percentage magnitude and phase of that harmonic, the purpose being the elimination of the harmonic difference between the *Target V* and the *Load V* signal. The term, *worst harmonic offender* refers to the harmonic that accounts for the highest harmonic error between the *Target V* and the *Load V* voltages. Having compensated for the first, the user manually resolves the error due to the next *worst harmonic offender* and so on down the line, until all harmonic offenders are resolved.

A *worst harmonic offender* is identified from the harmonic table or the phasor diagrams displayed on the ***Manual Feedback and Phasor Diagrams*** front panel of the Testing Station, as shown in Figure 5.5. The phasor for the *worst harmonic offender* is highlighted with a yellow circle and there is an "x" checked against that harmonic in the

harmonics table. After eliminating *worst harmonic offender*, subsequent harmonic offenders are identified and resolved the same way.

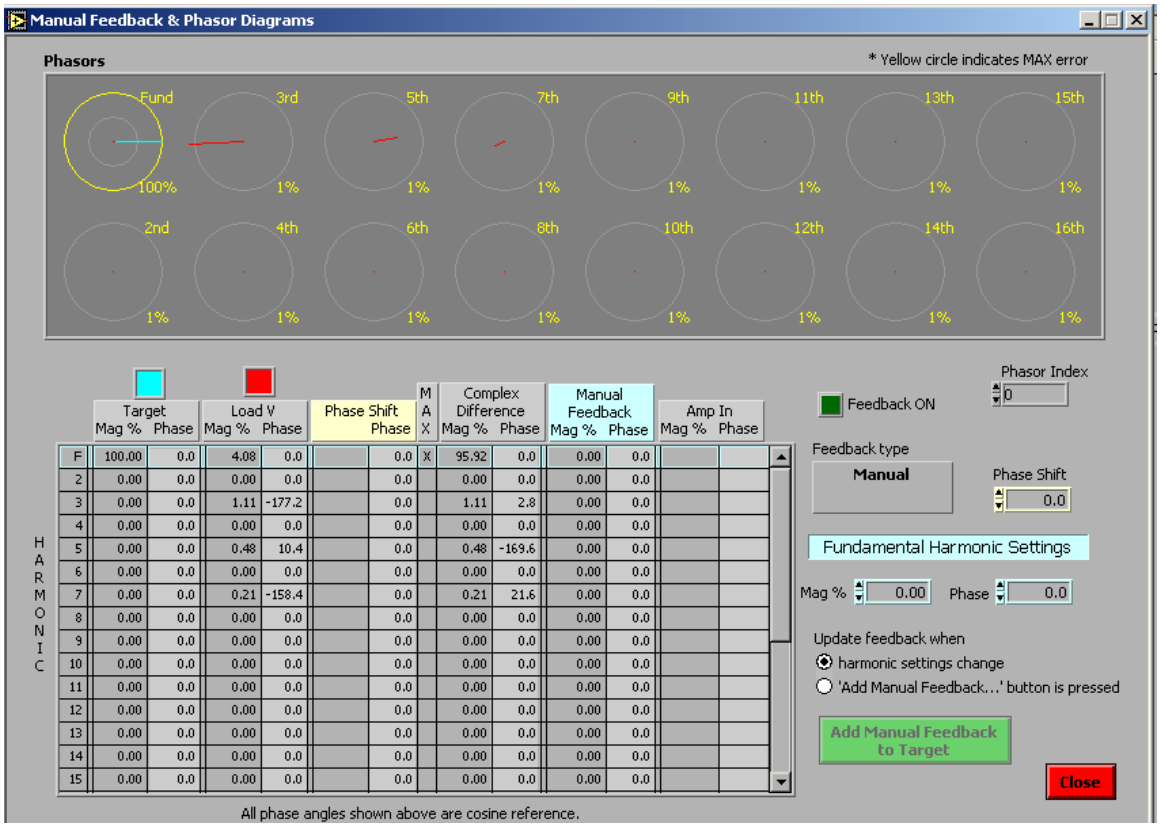



**Figure 5.5: Manual Feedback Operation Front Panel**

The process continues until all harmonics causing the error between the two signals are eliminated. The fundamental harmonic now remains as the one with highest magnitude, highlighted by its corresponding circular phasor, and the symbol "x" marked against it in the harmonic table.

In an ideal world, the fundamental signal is the original signal constituting *Load V,* and the only one that should exist. Our objective is to eliminate the undesirable

harmonic impurities present in the voltage potential at the PCC. The *Target V* Signal is the closest approximate expression of the ideal signal.

## 3. OPERATIONAL OVERVIEW OF THE TESTING STATION

The operation of the given system is a sequence of the following five steps:

### *I. Initialization*

When the Testing station is started up, the initial *AO* (analog output) waveform is generated. As we are at the beginning of the process, there is no feedback signal. The AO signal, therefore, is at its closest approximation to the reference *Target V* signal and contains the desired harmonic content. However, we will assume the system is operating with the feedback operation enabled for future iterations.

The content of the *AO* waveform data depends upon whether the *Testing Station* is employing, the *Stand Alone Mode* or the *Summing Junction Mode*. In the former, the *AO* signal entails the error-adjusted signal added to the *Target V* signal, in the latter mode, the *AO* signal is a sum of an external 60 Hz AC supply and the error-adjusted signal. The operational default will be *Summing Junction Mode*.

The *AO* waveform is then output from the Testing Station and input into a *Pulse Width Modulated* amplifier, representing the amplifier input or the *Amp-In* signal[8]. The amplifier processes the *Amp-In* signal is such a way as to create an amplifier output voltage within acceptable limits of harmonic distortion. The given amplifier output voltage appears across various non-linear loads as *Load V* the load voltage*,;* it also represents the voltage potential at the point of common coupling.

[8] In-depth discussion of the Pulse Width Modulated Amplifier is beyond the scope of this document.

### *II. Data acquisition of the Analog Input data:*

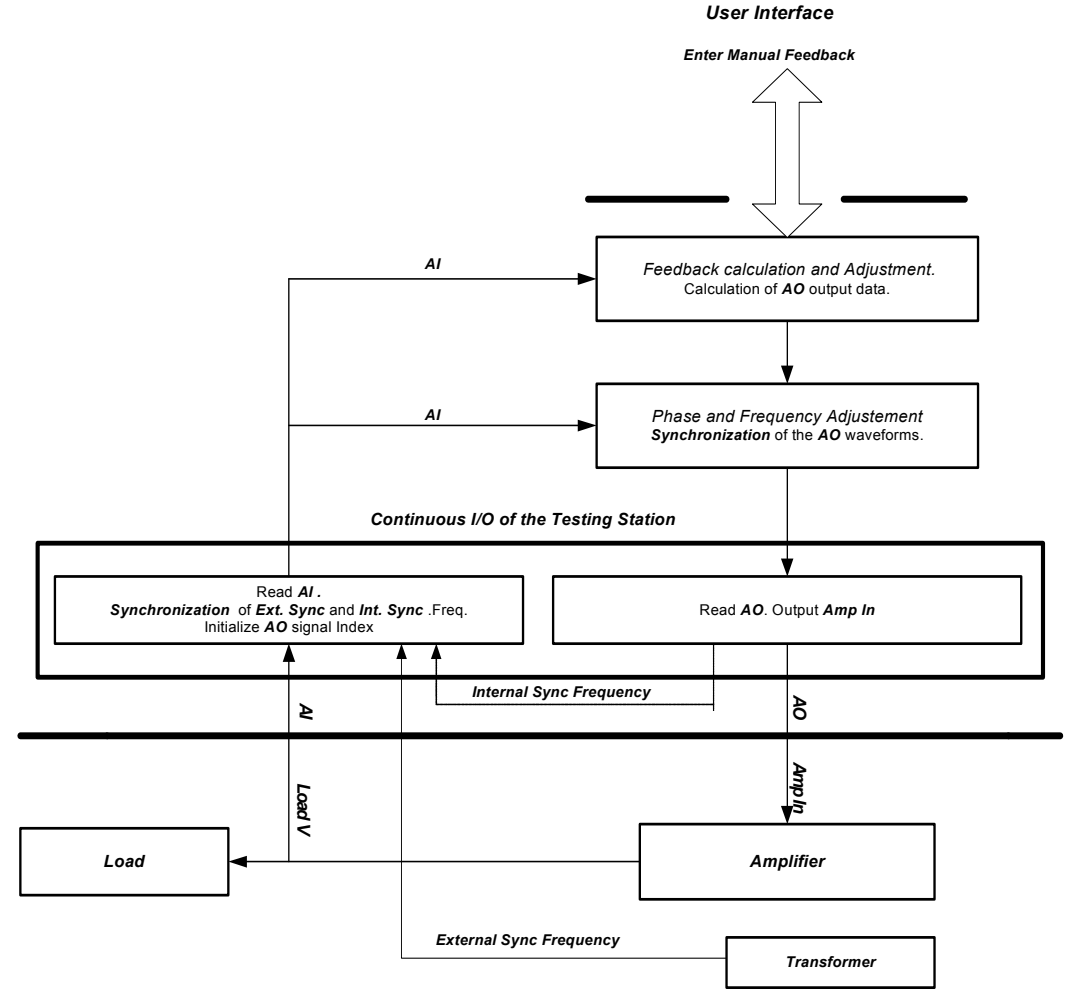
The *Load V* signal is input back into the Testing Station as the *AI* (analog input) signal through data acquisition. Hardware channels of a data acquisition device are dedicated to import the *AI* data into the Testing Station.

The *AI* data is a composite signal that consists of the following components:

- *Load V:* Load voltage signal
- *Load i:* Load current signal
- *External Sync Frequency signal:* 60 Hz frequency signal
- *Internal Sync Frequency signal:* The frequency signal representing the *AO* voltage signal of the previous iteration

The process of *AI* data acquisition involves the following steps:

- Memory (Buffer) Allocation: allocating a linear buffer to read the *AI* data.
- Writing the data into the allocated *AI* buffer




AI - Analog Input

AO -Analog Output

Amp In -AMplifier Input

**Figure 5.6: Block Diagram of the Testing Station**

### *III. Feedback:*

The objective of the feedback calculations for a given iteration is to generate a feedback signal that reduces the error between the *Target V* and *Load V* voltage.

Our goal is for the *Load V* voltage to match the *Target V* voltage in amplitude, phase, and harmonic content. The closer we can get the *Load V* voltage to the *Target V* voltage on these three factors, the easier it will be to contain the harmonic content of the *Load V* to within acceptable levels. Once we have corrected the *Load V* signal, we input it into the various loads such a personal computers, microwave ovens, etc in order to improve the efficiency of these devices.

The following sequence of steps describes a successful feedback operation (as shown in Figure 5.7):

- First we calculate the difference between the *Target V* voltage and the *Load V* voltage, then multiply with *Accel Factor (Mag%)* and *Accel Factor (Phase)* (or only the *Accel Factor (Mag%)* depending upon the feedback method employed). This is how we calculate the appropriate amount of feedback, labeled as the signal "*Feedback Applied"* in Figure 5.7.
- The *Feedback Applied* signal is added to the *Previous Feedback* signal to generate the *Feedback for the Current Iteration*. Then the *Feedback for the Current Iteration* is stored as the *Previous Feedback* signal for the next iteration.
- The feedback signal, once we have calculated it based upon our preferred operational mode– *Summing Junction Mode* or the *Stand Alone Mode*, is used to generate the analog output *AO* waveform data. The *AO* waveform output from the Testing Station is now labeled as the *Amp-In* (amplifier input) signal that is input into the amplifier.

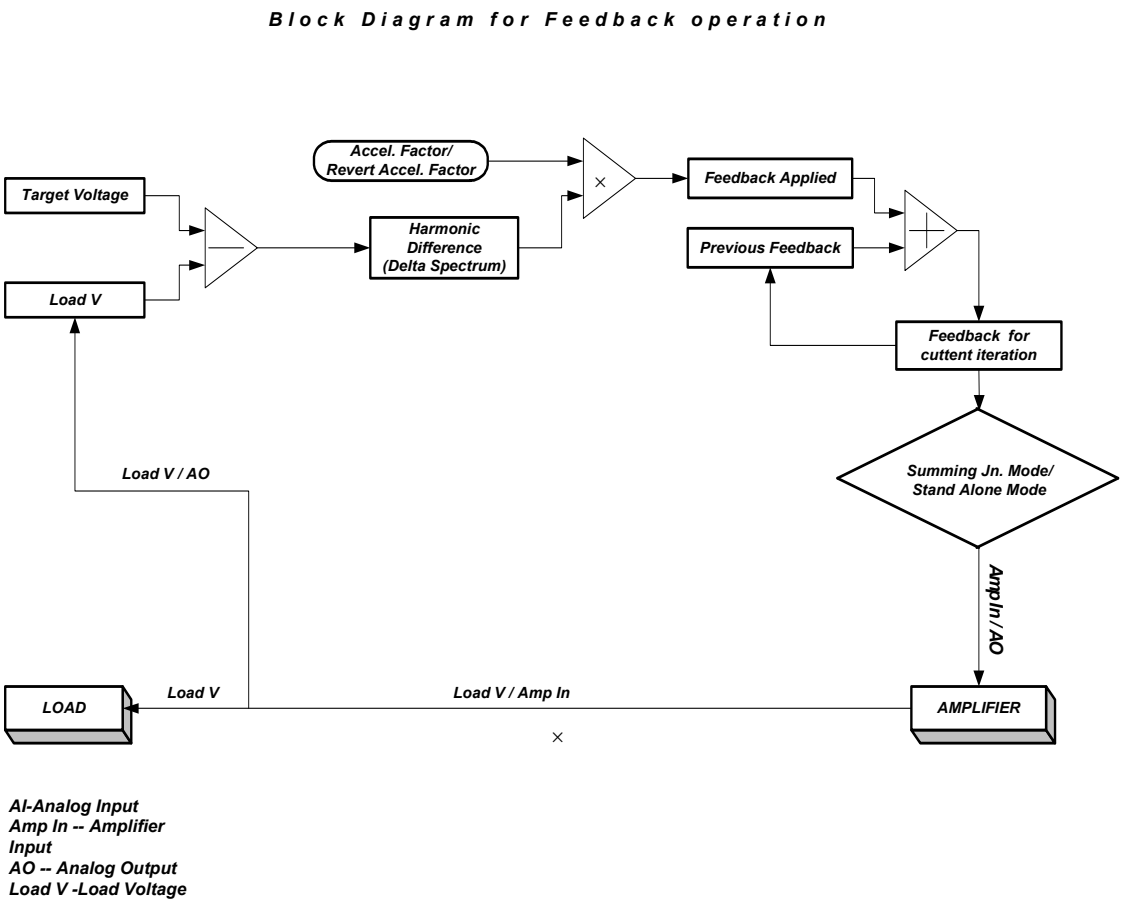



**Figure 5.7: Block Diagram of the Feedback Operation**

- The amplifier magnifies the *Amp-In* signal, up to an appropriate value, to generate the *Load V* signal.
- The *Load V* signal is then input into the Testing station as *AI,* the analog input signal used to calculate the feedback signal in the next iteration. At this point, the full cycle of the closed loop feedback operation is completed.

Five different methods are available in the Testing Station to calculate the feedback, and subsequently the *AO* spectrum. Of these, we have employed

*Manual Feedback Operation* for our investigations. A brief description for each method is given below:

- *Polar Maximum Amplitude Error:* The given method determines and eliminates the maximum error between the polar values (magnitude and phase treated separately) of the *Target V* harmonics, and the load voltage, *Load V* (*AI*) harmonics.
- *Maximum Amplitude Error:* This method uses the complex values of *Target V* and *Load V* to calculate and reduce the maximum harmonic error between the *Target V* voltage and *Load V*. As in the case of the *Polar Maximum Amplitude Error* method, the *Maximum Amplitude Error* identifies the *worst harmonic offender* and reduces it, while retaining its complex form.
- *Lowest Non-zero Harmonic Error:* This method reduces the difference between the *Target* spectrum and the *Load V* spectrum voltages at the index corresponding to the *least harmonic offender*. The *least harmonic offender* is the harmonic that accounts for the least percentage harmonic error between *Target V* and *Load V* voltage.
- *Overall Amplitude Error:* This method o reduces the overall difference between the *Target V* spectrum voltage and the *Load V* spectrum, although unlike the former two methods, this technique does not identify and reduce individual harmonic offenders.
- *Manual Feedback:* This method involves nullifying the *worst harmonic offender* by manually entering the percentage magnitude, and phase values (equal in magnitude and opposite in polarity) at that harmonic index. Having

compensated for the worst offender, the user then enters the data to reduce the next highest offender.

The *worst harmonic offenders* are identified from the harmonic table or the Phasor diagrams in the *Manual Feedback and Phasor Diagrams* front panel as illustrated in Section 1.2, Figure 5.5. The phasor for the *worst harmonic offender* is highlighted with a yellow circle and there is an "x" checked against that harmonic in the harmonics table. Once we enter the feedback, the next highest harmonic is highlighted in the same way.

This process continues until all the harmonic offenders have been reduced, upon which the fundamental now stands as the harmonic with the highest magnitude, highlighted by its corresponding circular phasor.

***Revert Feedback Operation:***

As the name suggests, the given feedback operation involves reverting the *Load V* signal. If a feedback operation causes the *Load V* to overcompensate, then the error between the *Target V* voltage and the *Load V* increases albeit in the different direction. For example, if the *Load V* overshoots the amplitude of the *Target V* voltage instrad of matching it, the error becomes a negative value in the opposite direction (assuming that the original difference between the *Target V* and *Load V* is considered a positive value).

In order to correct this error, the next feedback iteration reduces it and more accurately matches the *Load V* with the *Target V* voltage. The operation correcting the overcompensation is defined as the *Revert Feedback operation*. All the methods used for conventional feedback calculations, described above, are modified to conduct the *Revert Feedback Operation* calculations.

### *IV. Synchronization:*

The process of synchronization involves synchronizing the *Internal Sync Frequency* of the Testing Station with the *External Sync Frequency*, the objective being to generate a continuous *AO* signal output from the Testing Station.

The *External Sync frequency* signal is the basic 60 Hz AC supply, which differs from the *Internal Sync frequency* signal, defined as the fundamental frequency derived from the *AO* voltage signal generated during the last iteration. The two frequencies are used to determine the fundamental frequency of the *AO* harmonic waveform for the current iteration. This fundamental frequency is labeled as the new *Internal Sync Frequency* (used in the next iteration).This fundamental frequency is also used to determine the number of cycles of the fundamental signal.

The following entities constitute the composite *AO* signal and generate the *AO* harmonic waveform:

- Signal magnitude (entered by the user)
- Fundamental frequency
- Number of cycles for the fundamental signal
- *AO* signal array size

The *Internal Sync Frequency* serves as an internal clock to the Testing Station. It regulates the *AO* waveform output from the Testing Station ensuring that the *AO* data is output as a continuous stream of data and that each harmonic component of the *AO* signal is synchronized to the fundamental component of that signal, for that iteration, as shown in Figure 5.8.

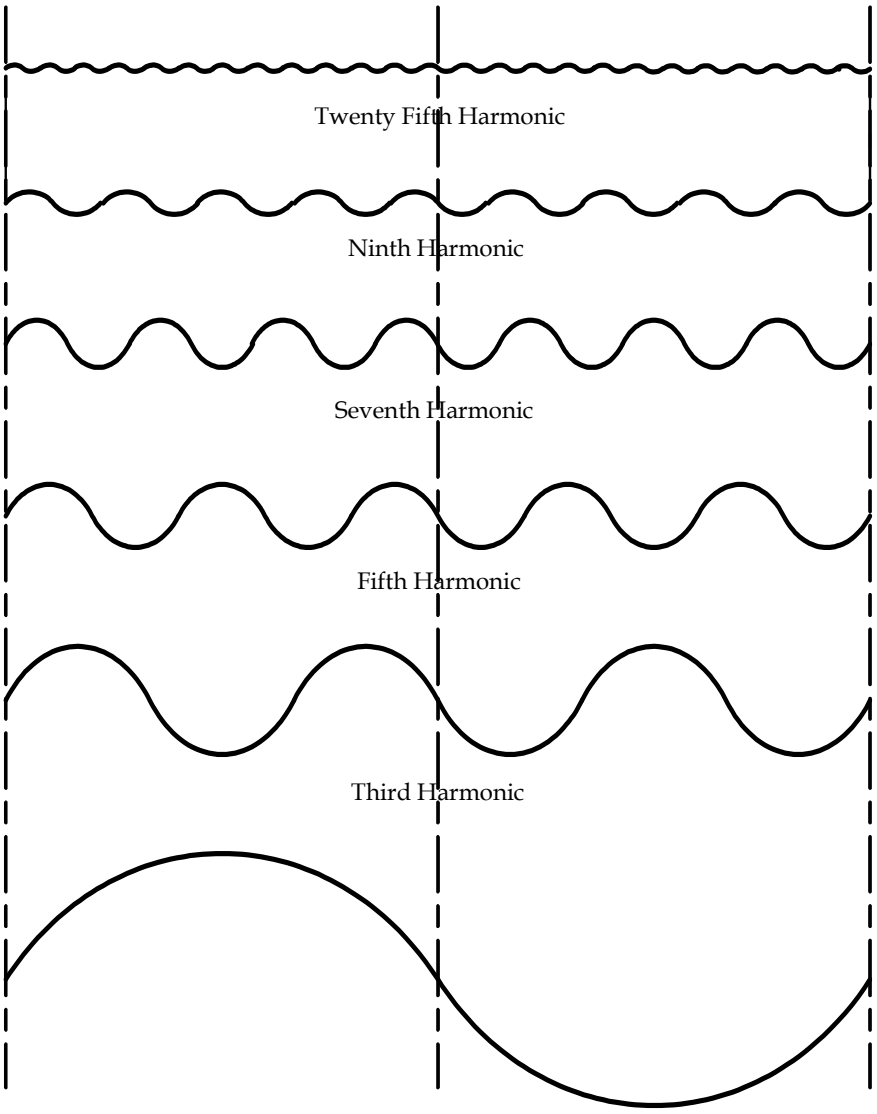



**Figure 5.8: Synchronizing Harmonics with the Fundamental**

The first step towards generating a continuous *AO* waveform is initializing the composite *AO* data, the fundamental signal, and its higher harmonic components at the same origin (as illustrated in Figure 5.8) during the current cycle. The initialization of the individual harmonic waveforms of *AO* waveform at a common Index requires that we

first synchronize, the *Internal Sync frequency* signal with the *External Sync frequency* signal. To do this, we need to calculatie the phase difference between the two frequencies and then shift the *Internal Sync Frequency* signal so that it is synchronized with the *External Sync Frequency* signal. Matching the two frequencies ensures that the fundamental frequency (or the new *Internal Sync Frequency*) of the *AO* signal is 60 Hz, and synchronous to a regular AC supply.

The two frequencies, the *Internal Sync Frequency* and the *External Sync Frequency* are monitored graphically on the *TEST STATION* front panel. A third frequency, the *Internal Adjustment Frequency* (representing the corrected, phase-shifted *Internal Sync Frequency* is also displayed simultaneously.

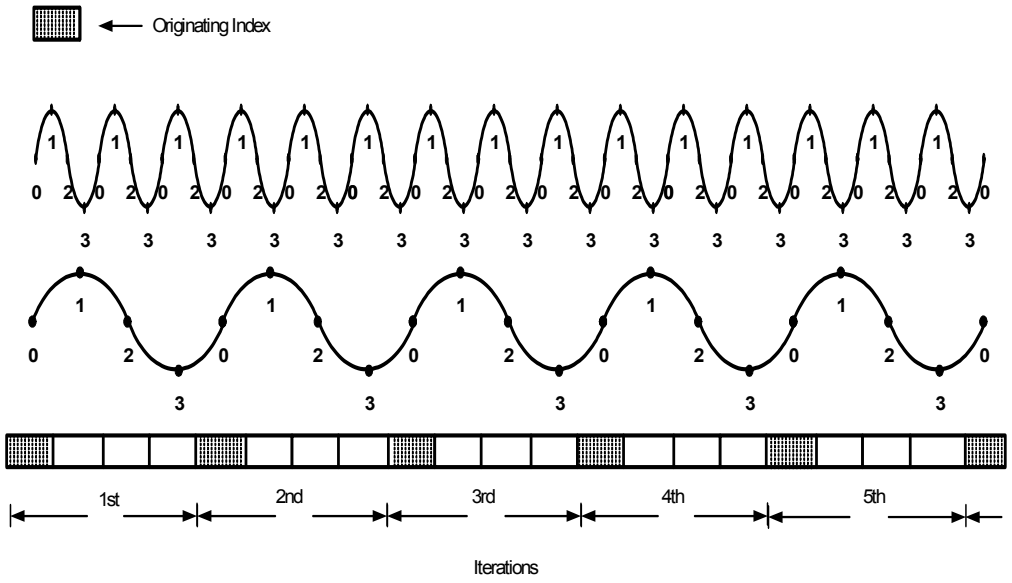



**Figure 5.9: Synchronization of Successive Waveforms to Form a Continuous Signal**

Once the fundamental frequency for a given iteration is determined, the *AO* waveform between successive iterations is synchronized in such a way that the waveform for a given iteration is truncated at the last index before crossing the zero level. This

enables the AO waveform of the next iteration to start at the zero-crossing index, thus ensuring that the *AO* waveform is continuous through all iterations, and that all harmonic cycles constituting the *AO* waveform signal for the current iteration are synchronized both to the fundamental, and as a logical consequence with each other. This description is shown in Figure 5.9.

The phase-adjusted *Internal Sync Frequency* is then fed back into the system so that the *AO* waveform for the next iteration is also initialized at the same index, according to the phase-adjusted *Internal Sync Frequency*. This further ensures that the *AO* waveform of the next iteration is contiguous to the waveform of the current iteration.

### *V. Output of the AO data:*

Once created, the *AO* waveform signal is written into a circular buffer array, as shown in Figure 5.10, and it is output from the testing station. The circular buffer economizes the buffer memory used to store the *AO* waveform signal array by recycling it, i.e. using the same memory space repeatedly to store successive *AO* waveform data.

Successful implementation of the *AO* buffer is based upon the principle that the rate at which the *AO* waveform signal is output from the buffer is synchronized with the rate at which it is written into the array. The *AO* waveform signal is output at a constant rate, but the rate at which it is written into the buffer depends upon the Testing Station's system speed. The two processes should be synchronized to prevent any *AO* data corruption, and to ensure efficient use of the memory.

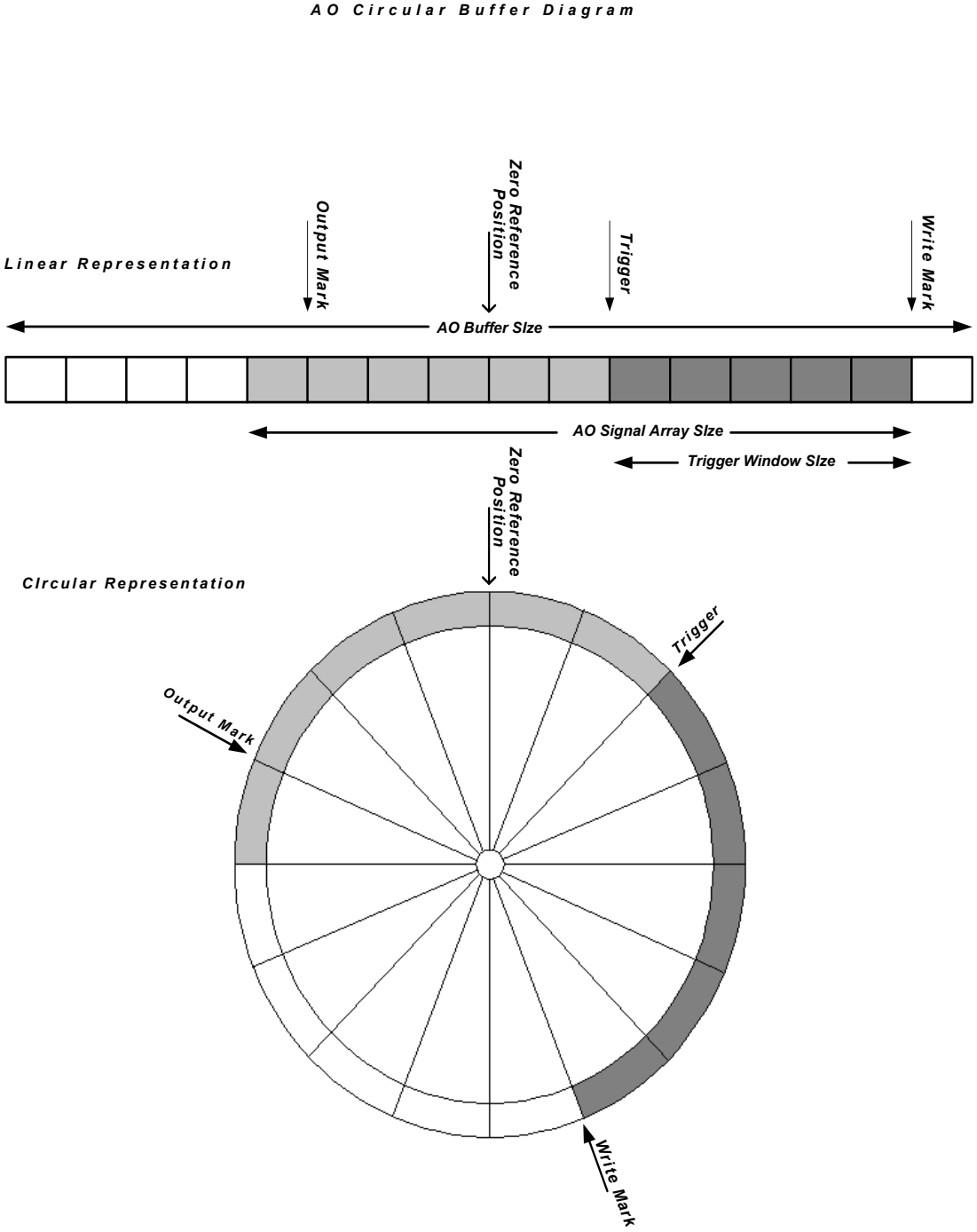



**Figure 5.10: Output of AO Data Using a Circular Buffer Memory**

The *AO* waveform signal output from the Testing station is fed to the amplifier as the *Amp-In* signal. The content of the *Amp-In* signal depends upon the mode of operation of the Testing station. If the Testing Station is in:

- *Stand Alone Mode,* then

$$Amp - In\ Signal = AO\ Signal = Target\ V\ Voltage + Feedback\ Signal$$

If in:

- *Summing Junction Mode,* then

$$Amp\ In\ Signal = AO\ Signal + External\ Voltage(60\ Hz\ AC\ supply)$$

The amplifier processes the *Amp-In* signal to generate the *Load V* containing the desired harmonic levels. The corrected *Load V* is fed into system as the *AI* input signal and the next iteration begins.

## 4. VALIDATING THE PROPOSED ANALYTICAL CIRCUIT MODEL

The proposed equivalent circuit model is an aggregation of all the single-phase power electronics loads connected at the PCC of a distribution feeder network and powered by a sinusoidal voltage source with user-defined harmonic content. Individually, each single-phase power electronics load behaves as a small harmonic current source, adding a minute current into the main supply; by simulating all harmonic current-injectors connected at the PCC collectively, as a single source, the equivalent circuit model combines their individual contributions into a single composite harmonic signal.

This response of the equivalent circuit model finds expression in the mathematical representation of composite harmonic current signal, labeled as, $I_{S,MOD}$. For a sinusoidal harmonic voltage, theoretical determination of $I_{S,MOD}$ offers us an ability to predict the extent of harmonic aggravation, of both voltage and current at the PCC that will actually occur. This information will help us analyze the interdependence between the harmonic

distortion in the voltage at the PCC and main supply current. This offers us a significant advantage in that we are able to monitor, and proactively contain harmonic regression of both the voltage at the PCC and the main supply current in a real physical scenario.

The Testing Station can be viewed as the experimental equivalent of our proposed analytical model. It too simulates the conditions at the PCC with N single-phase power electronics loads connected to it. The analytical model, for a given harmonic voltage input, generates a theoretical response $I_S$ and a unique solution of the parameters ($C$, $R_L$, $R_T$ and $L_T$ that define the equivalent circuit) collectively labeled as the *Correction Factor*. The model is considered valid if the current $I_S$ and the *Correction Factor* are consistent with the harmonic response of multiple single-phase power electronics loads connected to the Testing Station.

The methods of feedback and optimization employed in the *Harmonics Testing Station* share with our proposed *Response Optimization* algorithms the goal of – predicting and optimizing the harmonic current supplied to the distribution feeder network. Hence, we can employ the Testing Station to evaluate the performance of the *Response Optimization* algorithms, and the accurate modeling of the equivalent circuit.

## 5. EXPERIMENTAL APPLICATION OF THE HARMONICS TESTING STATION

We simulate an experiment with a composite load connected to a harmonic voltage source, by connecting that load to the *Harmonics Testing Station*. The results of that experiment show the accuracy of the equivalent circuit model in terms of its response, $I_S$, the input current pulse. These results also demonstrate the utility of the *Harmonics Testing Station* as a tool to benchmark the response of the proposed equivalent circuit model.

A composite load, made up of a – combination of a linear 60 Hz load and the power electronics load, was connected across the equivalent circuit model after which its load response was analyzed. Two components, the $I_L$ (linear) and the $I_{NL}$ (non-linear) loads, corresponding to the contributions of each constituent load, make up the input current pulse, $I_{COMP}$ The non-linear component, $I_S = I_{NL}$, was extracted from the composite load response. An initial estimate of the circuit parameters was optimized to a *Correction Factor* such that a modeled load response $I_{S,MOD}$ matched its physical equivalent $I_{S,MEAS}$.

We generated the data used to create the composite load waveforms using the *Harmonics Testing Station*. When the same load was connected to the Testing Station, we were able to reproduce the optimized response the input current $I_S$ of the power electronics portion of the composite load,thus, verifying and validating the accuracy of the proposed *Response Optimization* algorithms through the *Harmonics Testing Station*.

# CHAPTER 6

# Experimental Verification of *Response Optimization* Algorithms

## 1. INTRODUCTION

The algorithms we proposed in Chapter 4 should enable us to accurately predict the magnitude and nature of the harmonics (flatness or peakiness of the waveforms) injected back into a distribution feeder network by a multitude of single-phase power electronics loads connected to the network at the point of common coupling (PCC).

As shown in Figure 6.1, our equivalent circuit model is – an aggregate of the multiple loads connected to the distribution feeder network and powered by a harmonic supply voltage. The equivalent circuit can be modeled to represent either a single load connected to the PCC or a collection of such loads. The difference lies in the values of the circuit parameters that define the circuit.

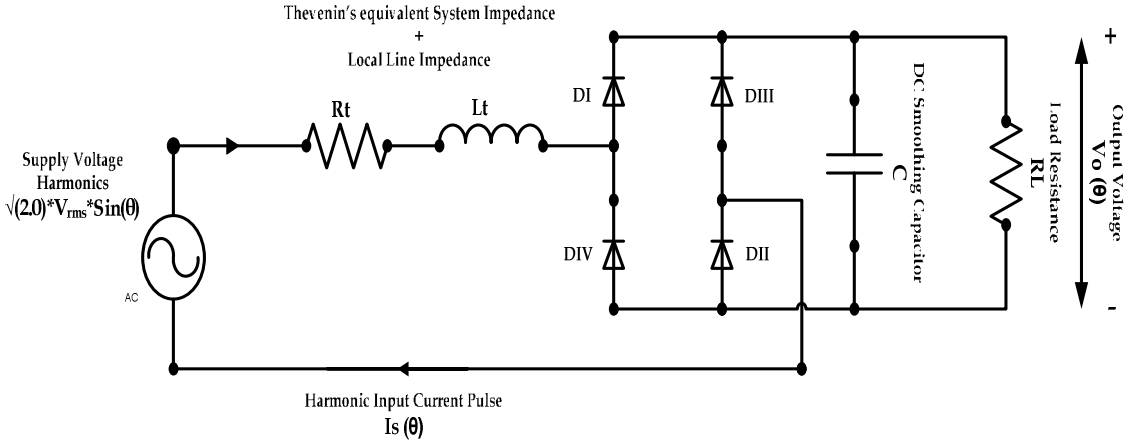



**Figure 6.1: Equivalent Circuit Model of Single-Phase Power Electronics Loads Connected to an AC Supply at the Point of Common Coupling**

A mathematical equivalent of the circuit model was derived as a function of the Supply Voltage $V_{IN}$, and the circuit parameters, consisting of the Discharging Capacitance $C$, the Load Resistance $R_L$, and the System Impedance $R_T$ and $L_T$. A

theoretical response of the equivalent circuit is mathematically expressed , in terms of the input current pulse $I_S$. $I_S$ charges the capacitor-filter of the diode-bridge rectifier component of the equivalent circuit model.

The algorithms as we have described them therefore perform the following tasks:

- They simulate the response of the equivalent circuit, i.e. they theoretically generate an input current pulse $I_S$ that flows through the equivalent circuit model as it is powered by a sinusoidal voltage source with a user-defined harmonic content. The *Load Response* algorithm is employed for this purpose.
- The modeled response, $I_{S,MOD}$ is then compared to, $I_{S,MEAS}$, its physical equivalent. Applying an *Error Calculation* algorithm, we generate the difference between the two responses.
- Finally, we use an *Error Optimization* algorithm to correct the simulated response $I_{S,MOD}$ so that it matches the physical response $I_{S,MEAS}$ to the maximum attainable accuracy. In the process, the algorithm optimizes the circuit parameters, $C$, $R_L$, $R_T$ and $L_T$ in order to yield the corrected simulated response for any harmonic voltage input. The parameters, therefore, give us the closest approximate representation of a physical circuit that would generate the optimized reference response $I_{S,MEAS}$. Collectively, these optimized set of values are labeled as the *Correction Factor*.

The present chapter will demonstrate the optimization procedure described above in different situations with different experimental constraints. We will present several scenarios, each of which, under a particular constraint, benchmarks the accuracy of the simulated response against its physical equivalent. Together, they demonstrate the robustness and viability of optimization algorithms in various situations. The following scenarios are presented in this chapter:

- *Scenario I:* Response Optimization with varying harmonic content in the Supply Voltage
- *Scenario II:* Response optimization with phase variation in the harmonic Supply Voltage
- *Scenario III:* Response optimization with a varying load $P_L$ connected to the equivalent circuit.
- *Scenario IV:* Response optimization with a varying *X/R* ratio of the equivalent circuit
- *Scenario V:* Special Cases
- *Scenario VI*: Response optimization for a composite power electronics load connected to the distribution feeder network.

### 2. SCENARIO I: RESPONSE OPTIMIZATION WITH VARYING HARMONIC CONTENT IN THE SUPPLY VOLTAGE

*Scenario Description:* The supply voltage to the circuit is a 120 $V_{RMS}$ sinusoidal voltage. We varied the harmonic content of the supply voltage to model several experimental scenarios. The first case is a pure sinusoidal supply voltage input to the equivalent circuit. The 3$^{rd}$, 5$^{th}$ and the 7$^{th}$ harmonics are subsequently added separately to the sinusoidal voltage, and upon each supply voltage variation we perform a simulation. Figure 6.2 shows the harmonic variations in the supply voltage input. Load $P_L$ connected to the equivalent circuit at 100W while the *X/R* ratio was held constant at 0.5, which it remained throughout the analysis. Experimental set-up for individual cases for Scenario I is listed in Table 6.1.

| Harmonic # | % Distortion | Phase | PL | X/R |
|---|---|---|---|---|
| *THDI* | 0.4 | 0 | 100 | 0.5 |
| *3* | 5 | 0 | 100 | 0.5 |
| *5* | 5 | 0 | 100 | 0.5 |
| *7* | 5 | 0 | 100 | 0.5 |

**Table 6.1: Experimental Set-Up for Individual Cases in Scenario I**

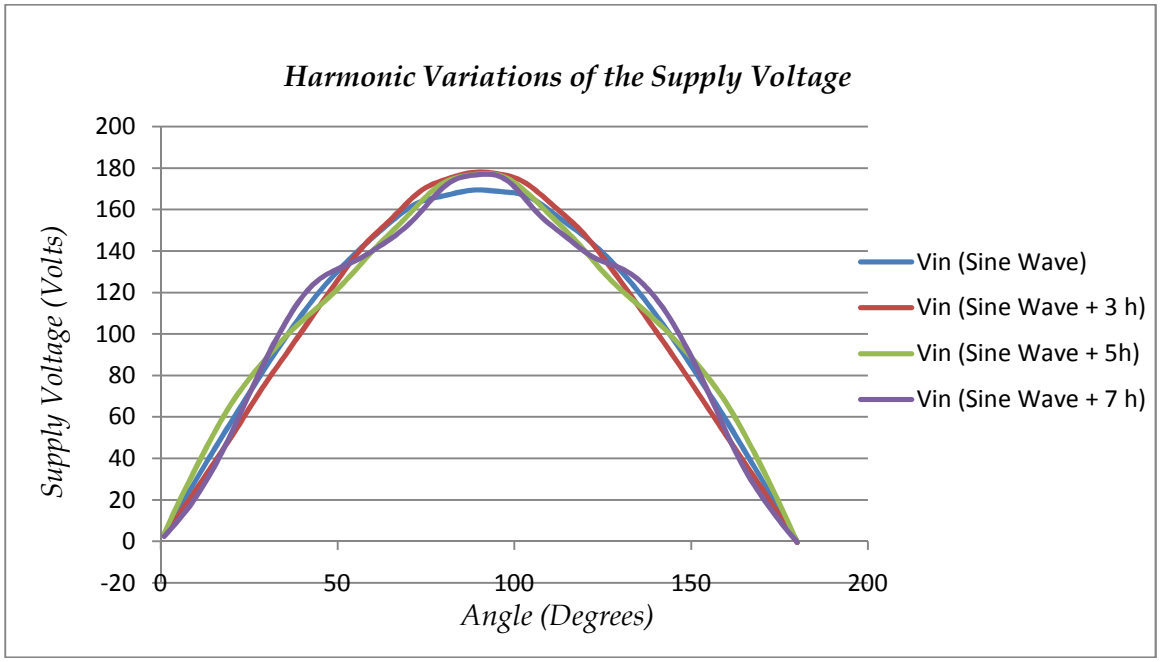



**Figure 6.2: Supply Voltage Curves with Varying Harmonic Content**

*Observations:* The objective of this experiment was to test the accuracy of the simulated optimized response of the equivalent circuit, when it was powered by a supply voltage of varying harmonic content. Individual harmonics were added to the supply voltage, and the effect of distortion caused by each harmonic separately was observed on the performance of the equivalent circuit.

Table 6.2 summarizes the results for Scenario I. It compares the difference, $E_I$, between, $I_{S,MOD}$ the optimized modeled input current pulse and its reference physical equivalent, $I_{S,MEAS}$.Our initial estimates of the circuit parameters, $C$, $R_L$, $R_T$ and $L_T$ and their final optimized values are collectively labeled as the *Correction Factor*.

| Harmonic Response Data for Varying Harmonic Supply Voltage | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| h[9] | $E_I$ | | C | | $R_L$ | | $R_T$ | | $L_T$ | |
| | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* |
| *1* | 599.53 | 12.39 | 1091.81 | 196.25 | 144.4 | 807.29 | 2.3 | 2.51 | 3.05 | 0.88 |
| *3* | 673.57 | 19.68 | 1100.22 | 202.08 | 144.14 | 876.84 | 2.21 | 2.55 | 2.93 | 0.88 |
| *5* | 730.8 | 23.98 | 1118.12 | 256.55 | 143.92 | 884.2 | 2.07 | 2.22 | 2.74 | 0.64 |
| *7* | 762.55 | 18.61 | 1119.94 | 262.79 | 144.21 | 862.82 | 1.92 | 2.15 | 2.55 | 0.54 |

**Table 6.2: Optimized Solution of Circuit Parameters with Varying Harmonic Content in Supply Voltage**

In Figure 6.3 can be seen the harmonic response of the equivalent circuit, the simulated harmonic input current pulse, $I_{S,MOD}$, and its physical measured counterpart, $I_{S,MEAS}$.

Variations in the rectified output voltage, $V_O$, due to harmonic variations in the supply voltage are shown in Figure 6.4. Parameter variations – initial estimates and the final optimized values, are all illustrated for each circuit parameter in Figures 6.5 – 6.8 respectively.

[9] h in this case stands for harmonic component added to the Supply Voltage. h = 1 refers to the pure Sine wave; h = 3 refers to the 3rd harmonic added to the sine wave.

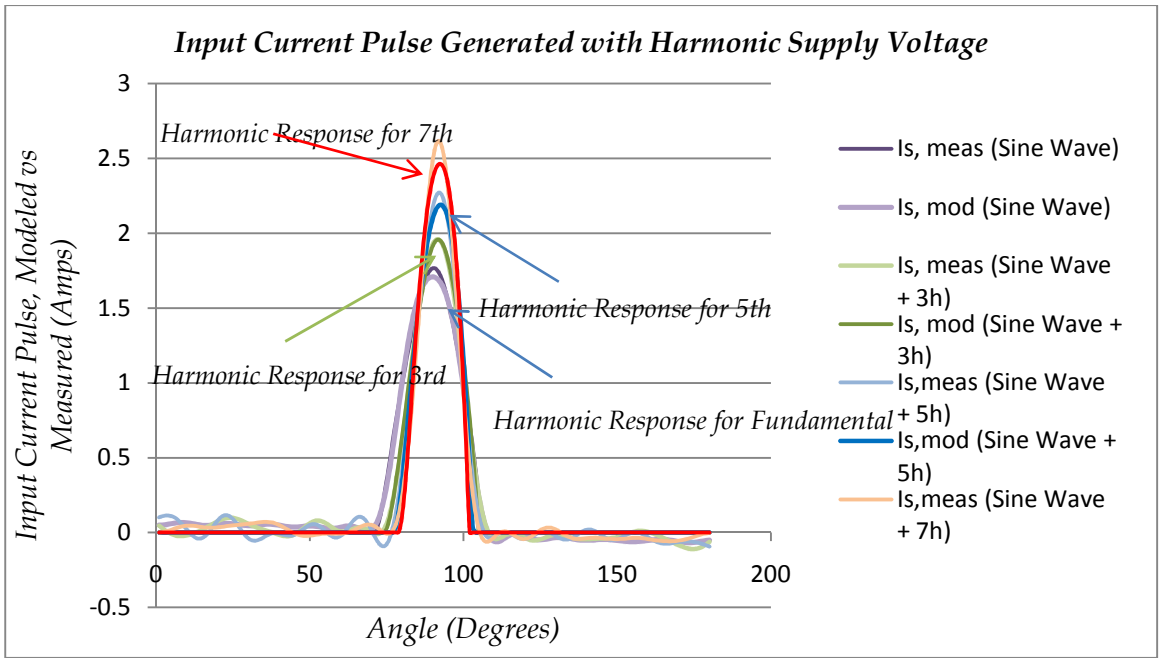



**Figure 6.3: Current Response for Varying Harmonic Content in Supply Voltage**

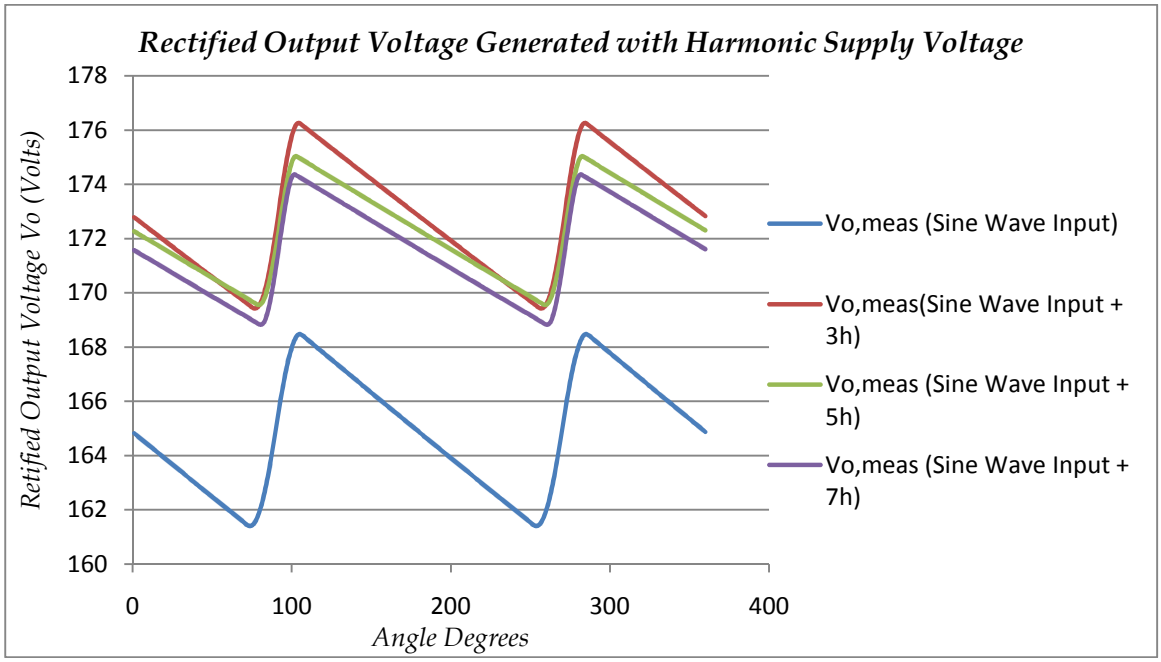



**Figure 6.4: Rectified Physical Output Voltage $V_{O,MEAS}$ for Varying Harmonic Content in Supply Voltage**

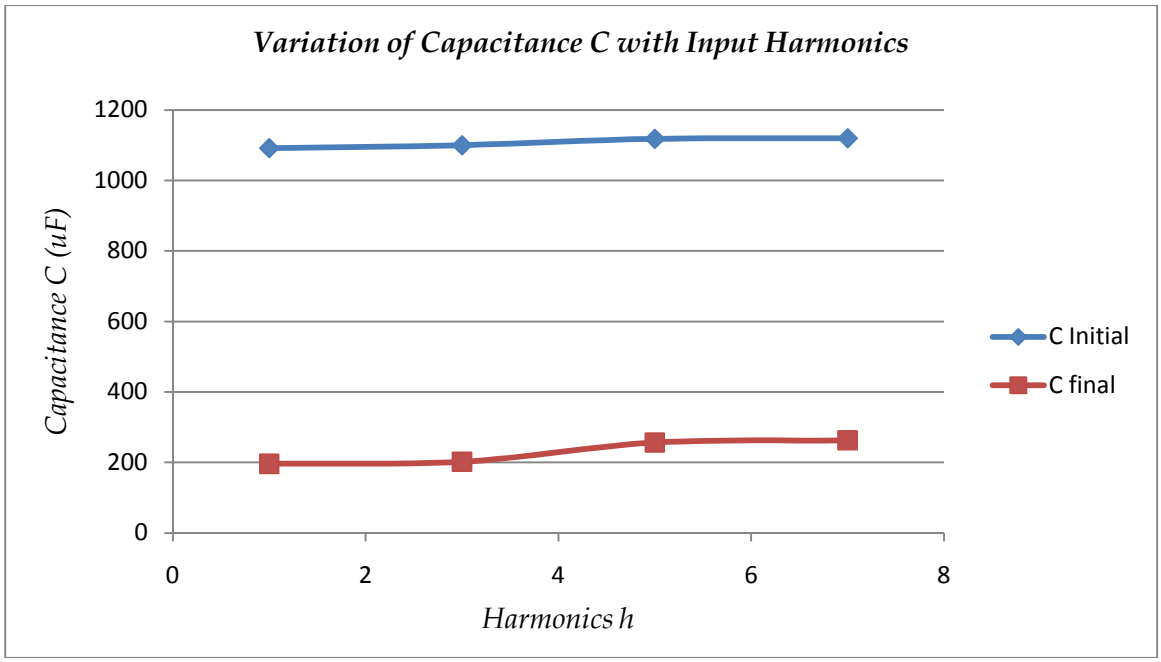



**Figure 6.5: Optimization of Discharging Capacitance C for Varying Harmonic Content in Supply Voltage**

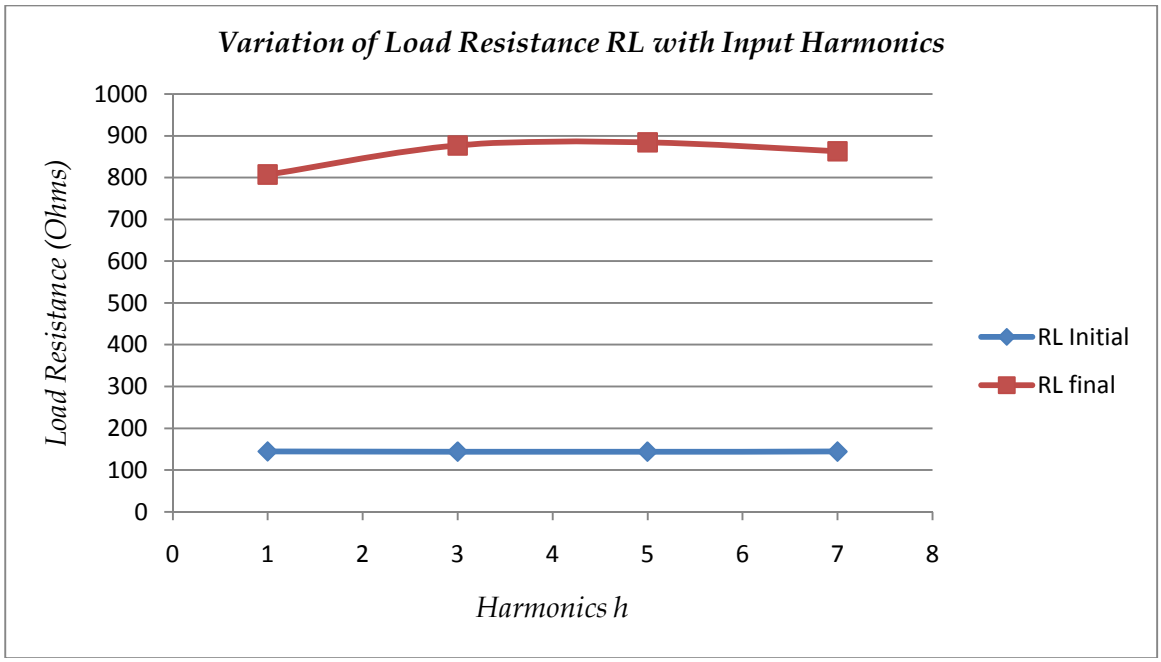



**Figure 6.6: Optimization of Load Resistance $R_L$ for Varying Harmonic Content in Supply Voltage**

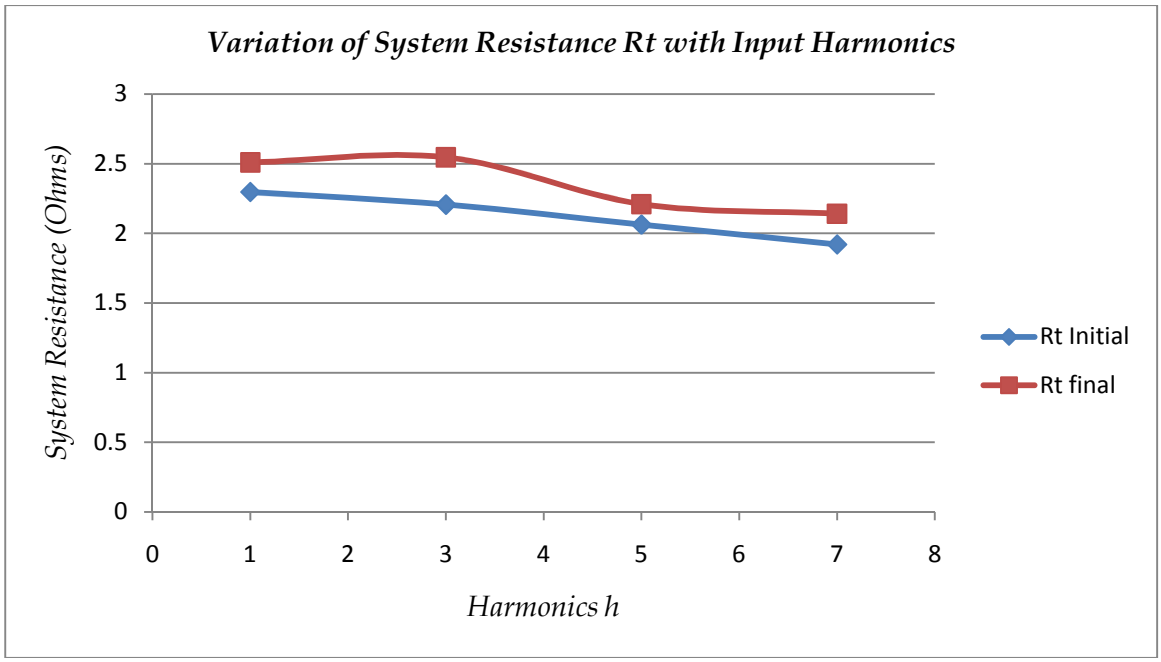



**Figure 6.7: Optimization of System Resistance $R_T$ for Varying Harmonic Content in Supply Voltage**

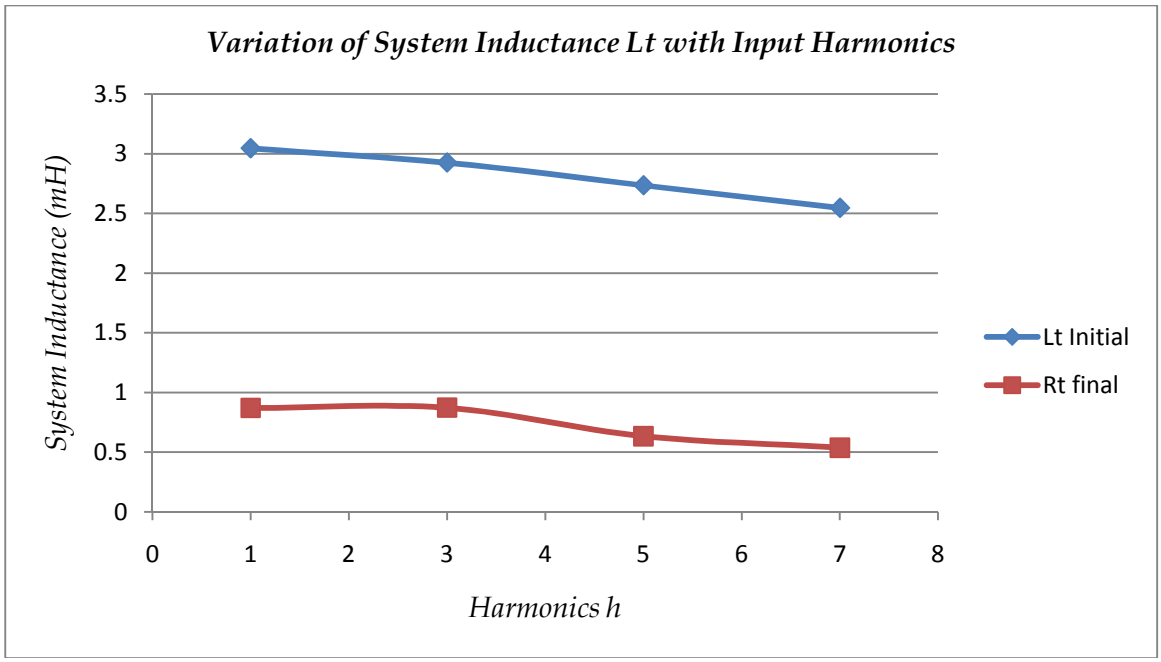



**Figure 6.8: Optimization of System Inductance $L_T$ for Varying Harmonic Content in Supply Voltage**

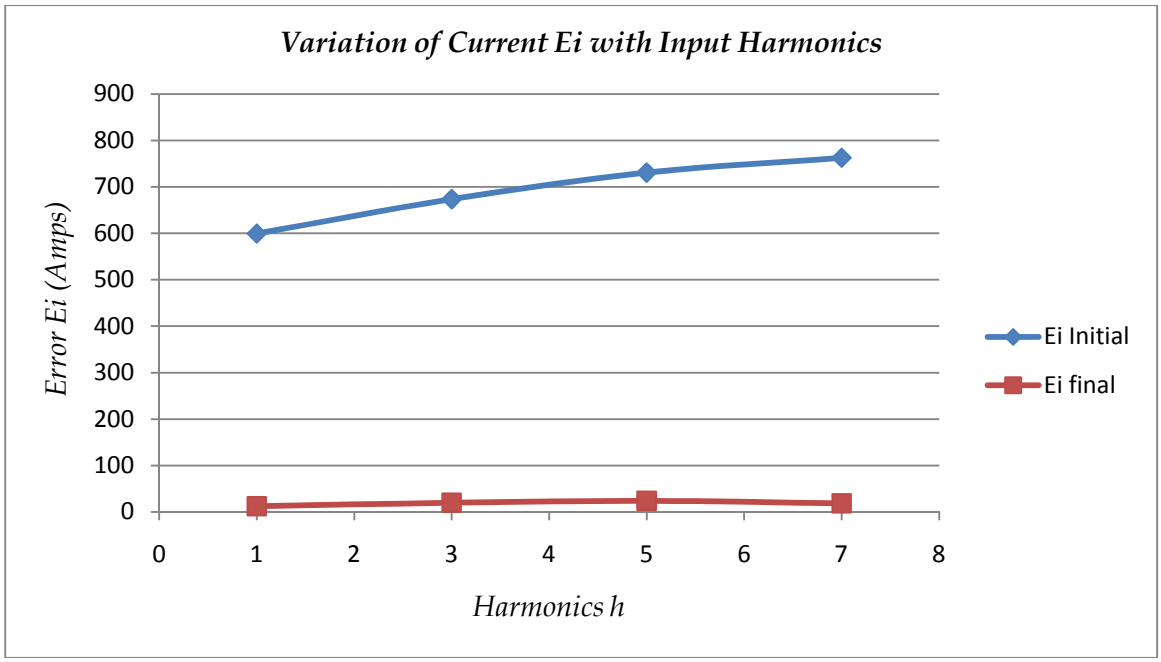



**Figure 6.9: Minimization of Current Error $E_I$ for Varying Harmonic Content in Supply Voltage**

*Conclusion:* The results in Scenario I lead us to the following conclusions:

- The circuit parameters converge to a common solution. Variation in the final optimized value of a circuit element (parameters: $C$, $R_L$, $R_T$ or $L_T$), between indivudal cases of the scenario is confined to a narrow range.
- The magnitude of the input current pulse increases with the addition of each higher harmonic to the supply voltage. In other words, the magnitude of the input current pulse is greater when the $7^{th}$ harmonic is added to the supply voltage than it is for the $5^{th}$ harmonic, which in turn will be greater than the current pulse generated for the $3^{rd}$ harmonic. Magnitude of the current pulse is observed to be the smallest for the fundamental. Table 6.3 lists the respective peak values of the physical (measured) and modeled input current pulses for different test cases analyzed in this scenario.

| Harmonic # | $I_{S,\,MEAS,\,PEAK}$ *(Amps)* | $I_{S,\,MOD,\,PEAK}$ *(Amps)* |
|---|---|---|
| *1* | 1.70 | 1.77 |
| *3* | 1.95 | 1.95 |
| *5* | 2.27 | 2.18 |
| *7* | 2.59 | 2.46 |

**Table 6.3: Comparison of the Peak Values of the Optimized Modeled Current Pulse $I_{S,MOD}$ and the Measured Physical Reference $I_{S,MEAS}$**

### 3. SCENARIO II: RESPONSE OPTIMIZATION WITH PHASE VARIATION IN HARMONIC SUPPLY VOLTAGE

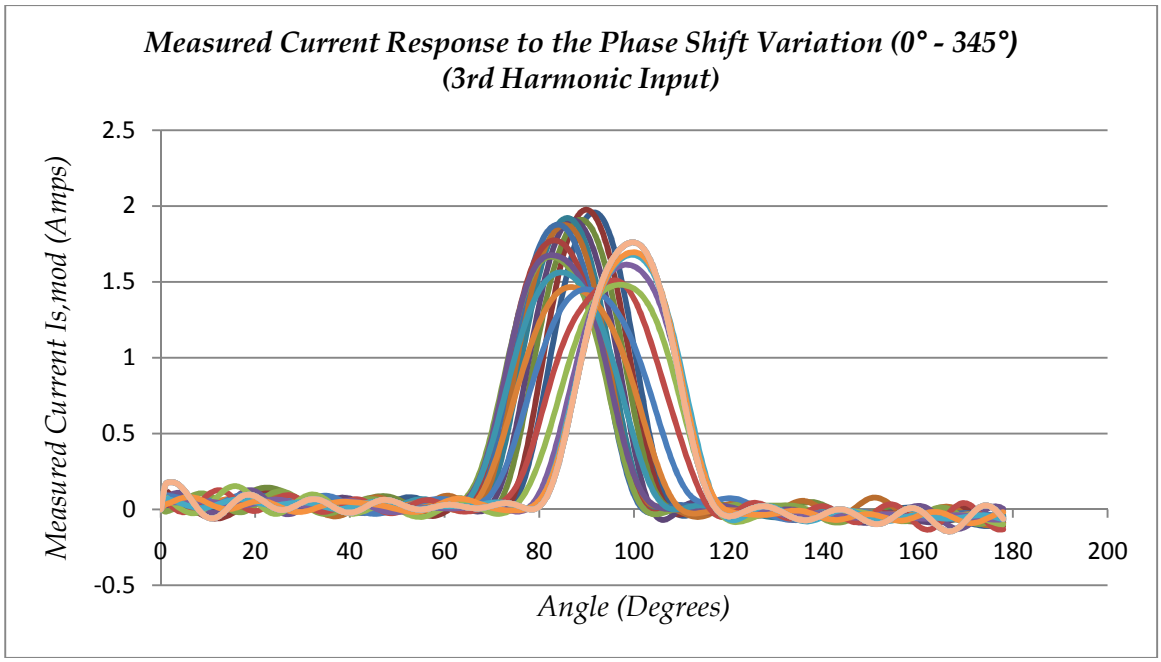
*Scenario Description:* The effect of phase-shift in supply voltage on the harmonic response of the equivalent circuit is observed in the following cases:

*Case I* – The equivalent circuit is powered by a 120 $V_{RMS}$ sinusoidal input voltage with 3rd harmonic distortion ranging between 4.8 – 5.1% added. We demonstrate the effects of phase-shift in the supply voltage waveform for a constant load $P_L$ = 100 W, and X/R ratio = 0.2 by varying the phase angle of the supply voltage in 15° increments traversing the entire 360° cycle. Table 6.4 summarizes the results for the given scenario. The table lists the difference, $E_I$, between the physical and the modeled input current pulse for each phase-shift increment, gives the initial estimates of the circuit parameters, $C$, $R_L$, $R_T$ and $L_T$ and lists their final optimized values for the proposed equivalent circuit.

| 1st Harmonic (X/R = 0.2, PL = 100W) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Phase Shift** | **$E_I$** | | **C** | | **$R_L$** | | **$R_T$** | | **$L_T$** | |
| | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* |
| *0* | 587.31 | 18.08 | 1100.22 | 317 | 144.14 | 876.58 | 4.42 | 2.85 | 2.35 | 0.58 |
| *15* | 589.51 | 23.71 | 1102.58 | 296.62 | 144.09 | 838.21 | 4.35 | 2.96 | 2.31 | 0.75 |
| *30* | 579.93 | 22.97 | 1103.07 | 347.68 | 143.94 | 861.05 | 4.37 | 2.89 | 2.32 | 0.61 |
| *45* | 572.13 | 18.62 | 1106.98 | 250.79 | 144.09 | 846.59 | 4.39 | 2.72 | 2.33 | 0.83 |
| *60* | 563.01 | 16.28 | 1104.84 | 242.33 | 143.98 | 837.53 | 4.38 | 2.63 | 2.33 | 0.82 |
| *75* | 545.98 | 25.07 | 1100.24 | 276.09 | 143.91 | 844.08 | 4.39 | 2.87 | 2.33 | 0.83 |
| *90* | 536.22 | 13.92 | 1093.97 | 271.69 | 143.94 | 820.88 | 4.4 | 2.64 | 2.33 | 0.74 |
| *105* | 512.53 | 15.09 | 1087.45 | 292.41 | 144.13 | 805.61 | 4.49 | 2.67 | 2.38 | 0.73 |
| *120* | 492.4 | 22.43 | 1093.05 | 190.09 | 143.7 | 819.45 | 4.67 | 2.4 | 2.48 | 1.15 |
| *135* | 470.03 | 22.19 | 1056.35 | 302.42 | 143.76 | 782.31 | 4.56 | 2.62 | 2.42 | 0.7 |
| *150* | 446.26 | 15.75 | 1080.33 | 225.61 | 143.95 | 768.15 | 4.77 | 2.81 | 2.53 | 1.14 |
| *165* | 433.6 | 14.22 | 1068.11 | 236.9 | 143.82 | 759.7 | 4.92 | 2.63 | 2.61 | 1.11 |
| *180* | 425.36 | 23.76 | 1068.85 | 209.75 | 143.81 | 761.11 | 4.91 | 2.72 | 2.61 | 1.33 |
| *195* | 440.04 | 20.98 | 1054.36 | 291.51 | 143.98 | 753.19 | 4.84 | 2.74 | 2.57 | 0.94 |
| *210* | 454.64 | 22.61 | 1071.7 | 254.65 | 143.97 | 758.02 | 4.85 | 2.63 | 2.58 | 1.07 |
| *225* | 440.04 | 20.98 | 1054.36 | 291.51 | 143.98 | 753.19 | 4.84 | 2.74 | 2.57 | 0.94 |
| *240* | 495.23 | 15.7 | 1083.81 | 281.12 | 143.8 | 767.29 | 4.56 | 2.69 | 2.42 | 0.82 |
| *255* | 518.96 | 19.97 | 1078.92 | 249.47 | 143.69 | 787 | 4.56 | 2.92 | 2.42 | 0.83 |
| *270* | 540.06 | 25.91 | 1100.15 | 294.42 | 143.92 | 804.24 | 4.49 | 2.81 | 2.38 | 0.75 |
| *285* | 549.12 | 26.01 | 1085.08 | 218.88 | 144.35 | 806.71 | 4.43 | 3.03 | 2.35 | 1.03 |
| *300* | 569.15 | 21.24 | 1097.45 | 293.11 | 144.01 | 837.57 | 4.43 | 2.89 | 2.35 | 0.7 |
| *315* | 569.75 | 18.87 | 1099.41 | 322.61 | 144.02 | 846.17 | 4.45 | 2.72 | 2.36 | 0.66 |
| *330* | 582.14 | 23 | 1096.29 | 250.05 | 144.43 | 881.52 | 4.4 | 2.56 | 2.33 | 0.74 |
| *345* | 582.02 | 22.24 | 1102.69 | 276.65 | 144.12 | 855.24 | 4.45 | 2.75 | 2.36 | 0.79 |

**Table 6.4: Optimized Solution of the Circuit Parameters with Varying Phase-Shift in Supply Voltage**

*Observations:* Figure 6.10 examines the progression in the input current pulse due to phase- shift variations in the input supply voltage when the 3rd harmonic is added to it. Both measured and modeled current pulse progression is illustrated.



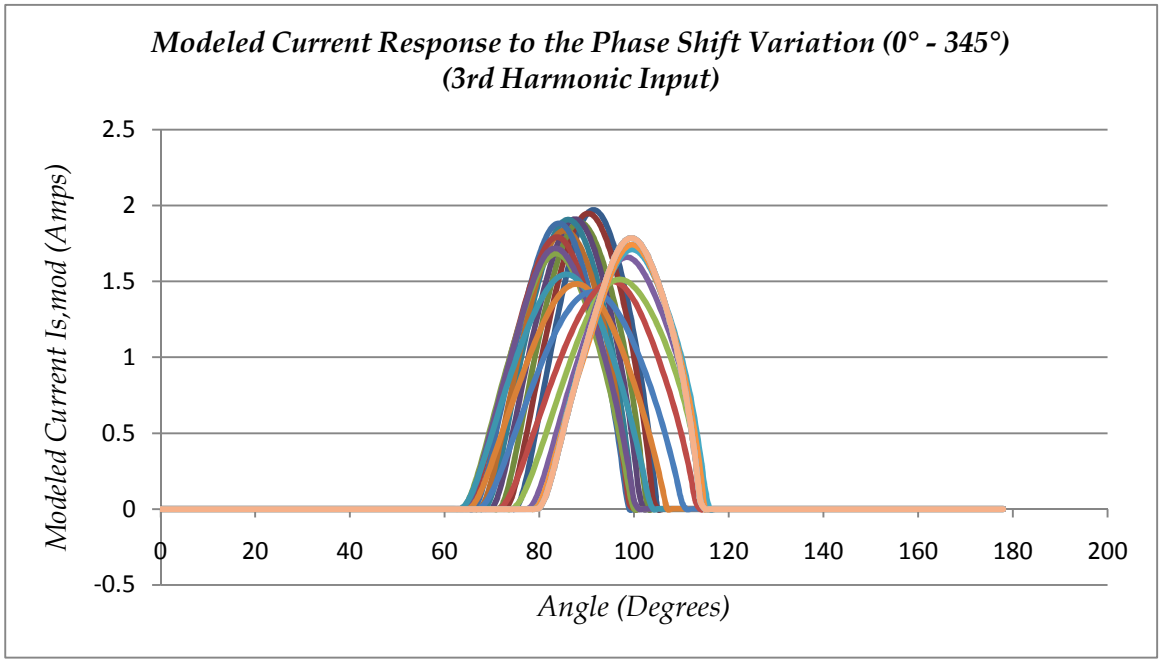




**Figure 6.10: Current Response Pulses $I_{S,MEAS}$ and $I_{S,MOD}$ with Varying Phase-Shifts in the Supply Voltage with 3rd Harmonic Added**

A sinusoidal voltage, phase-shifted by 90°, assumes a peakier shape, whereas the same input voltage waveform assumes a flattened shape under the application of a 180° phase-shift. A flattened voltage waveform will boreaden the current pulse at its base, creating a flattened current pulse, while a peakier voltage waveform tends to produce a peakier current pulse that is narrow at its base.

Our experiment shows that a flattened current pulse has less harmonic content than its peakier equivalent. Additionally, a broadened current pulse flattens the supply voltage waveform and further alleviates the harmonic content of the supply voltage. Hence a cyclical process is established that results in reduction of harmonic distortion in both signals.[10] Current pulse generated by a pure sinusoidal supply voltage has a peakiness comparable to the responses generated by the supply voltages being phase-shifted by 90° or 270°. However, the generated current pulse neither affects the shape (and hence the harmonic content) of the supply voltage, nor is affected in its shape un turn by the latter. [1]

Figure 6.11 shows examples of the 120 Vrms, 3rd harmonic input voltage with +/- 90° and +180° phase-shifts added to demonstrate the peakiness and the flattening of the voltage waveform compared to the supply voltage signal without any phase-shift.

Current pulses generated due to the peaky input voltage waveforms and the flattened voltage waveforms are compared to the current pulse generated by a supply voltage with no phase-shift in Figure 6.12.

[10] This phenomenon of mutual alleviation the harmonic content of the supply voltage and the resultant input current pulse finds application in the Partial Self-Compensation of the harmonic loads.

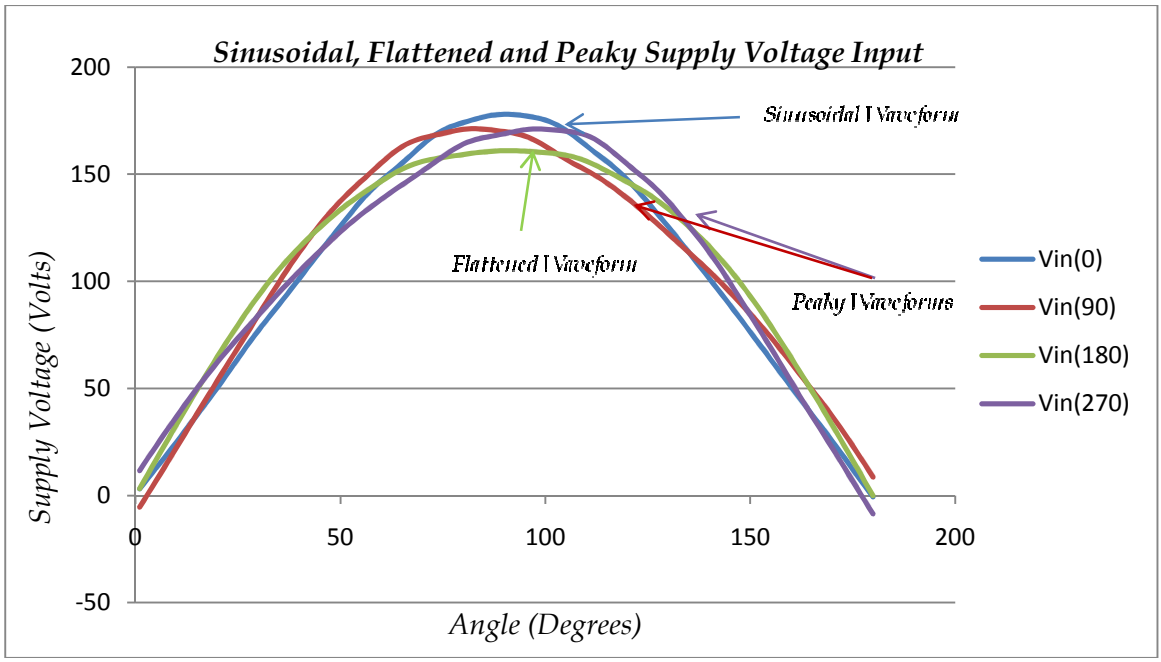



**Figure 6.11: Supply Voltage Curves with Varying Phase-Shift**

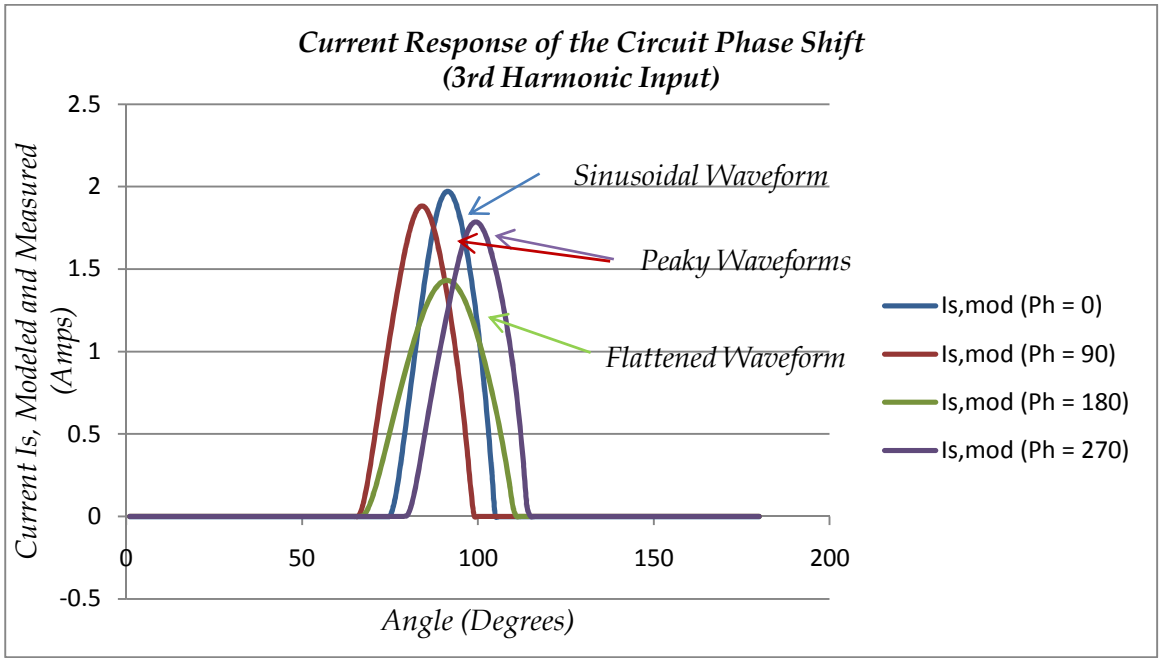



**Figure 6.12: Variation in Wave Shape of Current Pulse, $I_{S,MOD}$ with Varying Phase-Shifts in Harmonic Supply Voltage**

Figure 6.13 compares the magnitudes of the Fourier spectrum of the peaky (phase-shift = +/- 90°), flattened (phase-shift = 180°) and sinusoidal (phase shift = 0°) input current pulses. Magnitudes of the 3rd – 11th harmonics in the Fourier spectrum of the flattened current pulse are less than those of the peaky current pulse. It is also observed that the harmonic magnitudes of the current pulse for a pure sinusoidal supply voltage, is comparable to those of the peaky waveform. However, the peakiness of the current pulse does not affect the shape of pure sinusoidal voltage waveform, nor does the latter affect the shape of the former. Similar results were obtained for phase-shifts in supply voltages of different harmonic content.

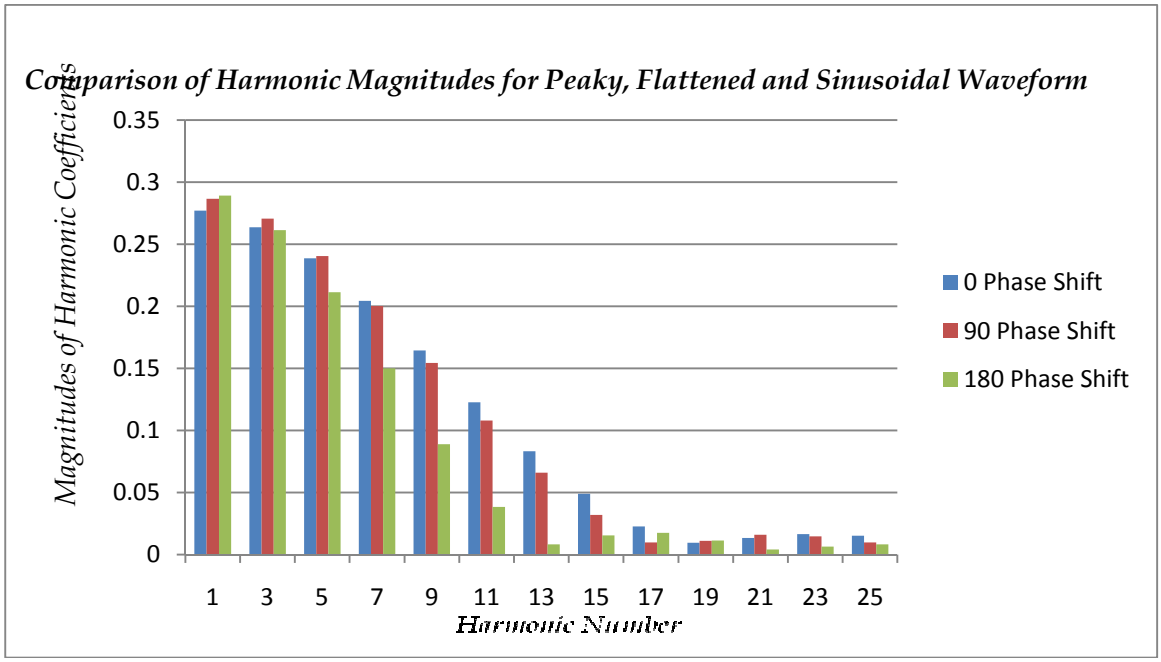



**Figure 6.13: Fourier Spectrum of the Current Response, $I_{S,MOD}$ for Sinusoidal (Ph = 0°), Peaky (Ph = 90°) and Flattened (Ph = 180°) Harmonic Supply Voltages**

Finally, Figures 6.14 – 6.17 illustrate the optimized solution resulting from theprogression and the final convergence of the parameters, $C$, $R_L$, $R_T$ and $L_T$ respectively,

to an optimized solution when the phase angle of the supply voltage input is varied in 15° increments for a complete 360° cycle. Our results indicate that, the parameters of the equivalent circuit model are independent of the phase-shift applied to supply voltage (with magnitude of the supply voltage unchanged), and thus converge within a narrow range.

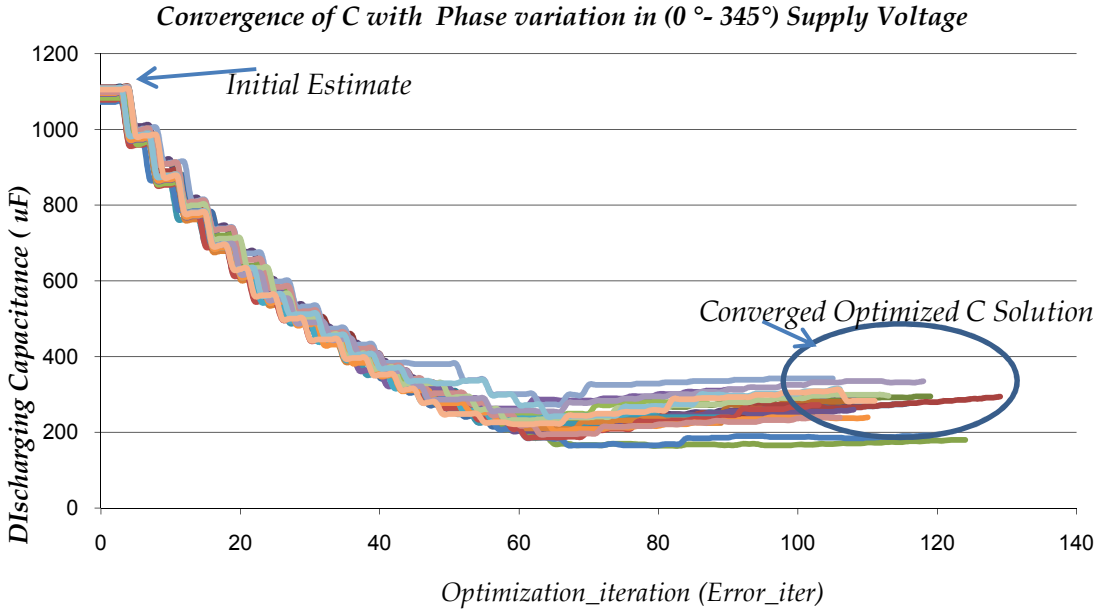



**Figure 6.14: Convergence of Discharging Capacitance C to a Common Optimized Solution for Varying Phase-Shifts (0° – 345°) in Harmonic Supply Voltage**

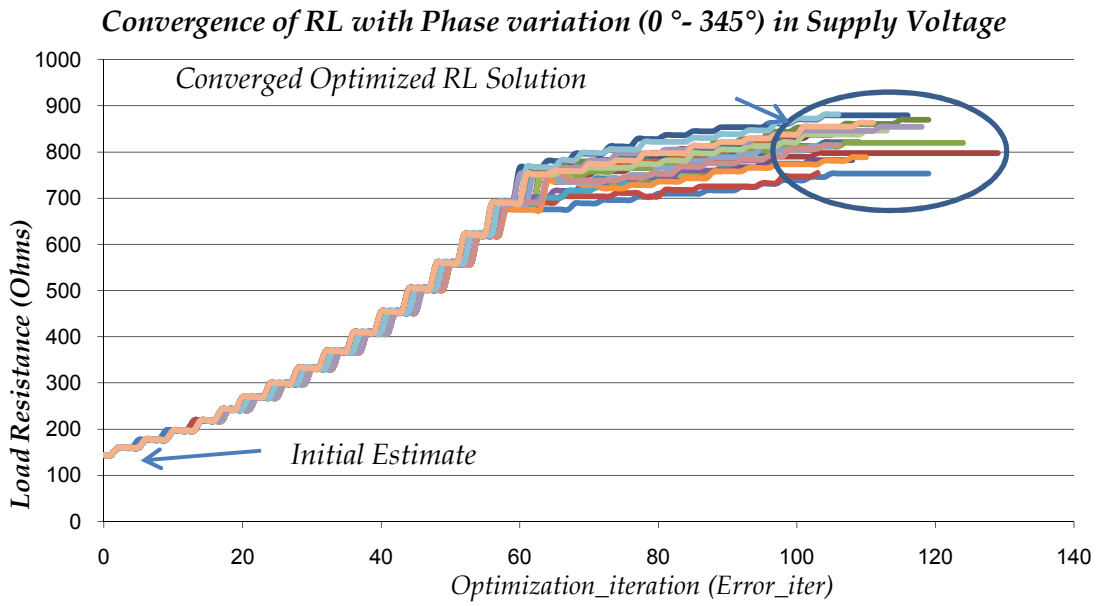



**Figure 6.15: Convergence of Load Resistance $R_L$ to a Common Optimized Solution for Varying Phase-Shifts (0° – 345°) in Harmonic Supply Voltage**

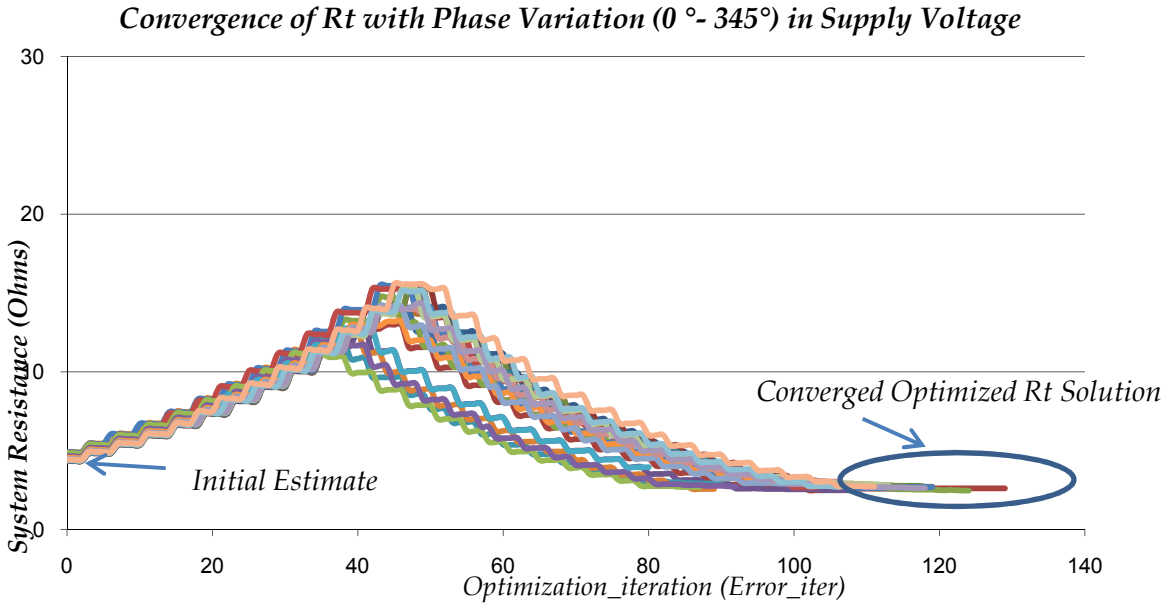



**Figure 6.16: Convergence of System Resistance $R_T$ to a Common Optimized Solution for Varying Phase-Shifts (0° – 345°) in Harmonic Supply Voltage**

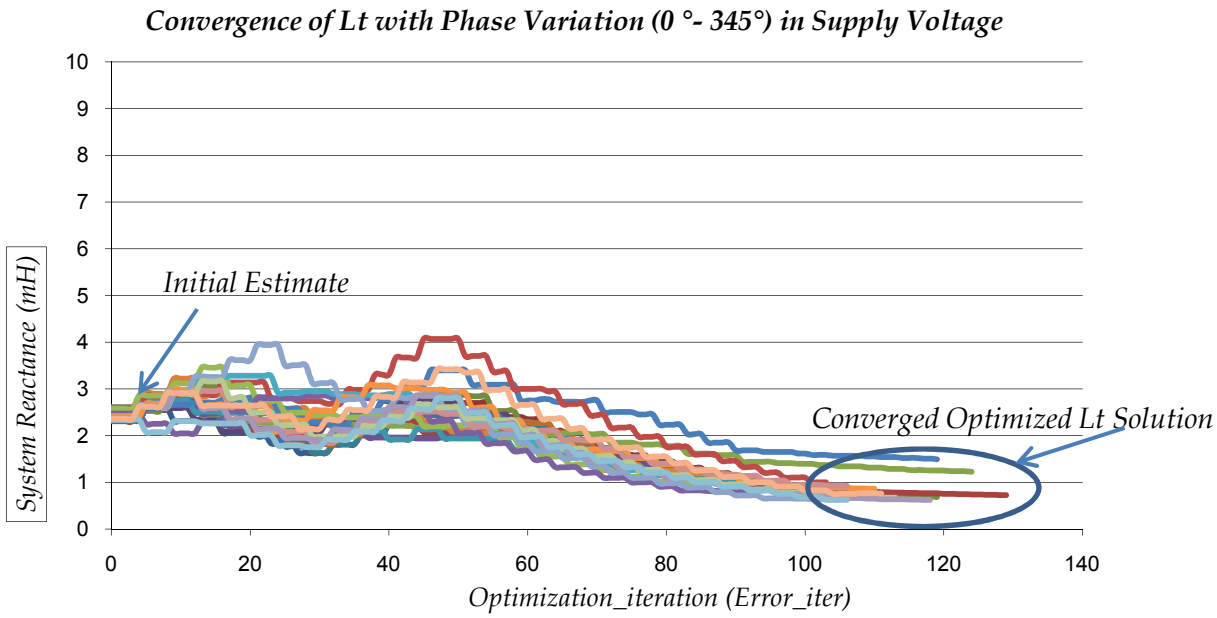



**Figure 6.17: Convergence of Load Inductance $L_T$ to a Common Optimized Solution for Varying Phase-Shifts (0° – 345°) in Harmonic Supply Voltage**

*Conclusions:* We can thus conclude that a flattened supply voltage waveform caused by a phase-shift of +/- 180° will create a flattened input current pulse (which naturally has reduced harmonic content) in contrast to a peakier current pulse with a narrower base, generated by the peakier version of the same voltage waveform phase-shifted by +/- 90°.

## 4. SCENARIO III: RESPONSE OPTIMIZATION WITH VARYING LOAD $P_L$ CONNECTED TO THE EQUIVALENT CIRCUIT

*Scenario Description:* In this scenario, a 120 Vrms sinusoidal voltage powers the equivalent circuit followed by the 3rd, 5th and 7th harmonic distortions respectively added to it. The phase-shift for each supply voltage input was maintained at 60° except for the fundamental which was simulated without any phase-shift in it. For a given supply voltage input, the circuit was simulated with a 50 W, 100W, 150W and 250 W load one time each, each being separately connected to it.

Variable load $P_L$ connected to the equivalent circuit generates an initial estimate of the load resistance $R_L$, as determined by the following equation:

$$R_L = V_{RMS}^2 / P_L \ldots (1)$$

This current scenario provides evidence for the fact that, in spite of varying initial parameter estimates, only one optimized solution exists for a given supply voltage input. This scenario, in addition, shows patterns of variation in each parameter due to a variable resistive load connected to the equivalent circuit. Experimental constraints for Scenario III are recorded in Table 6.5.

| Harmonic # | Vrms | | $P_L$ (Watts) | X/R |
|---|---|---|---|---|
| | Magnitude (V) | Phase (°) | | |
| *1* | 120 | 0 | 50, 100, 150, 250 | 0.5 |
| *3* | 120 | 60 | 50, 100, 150, 250 | 0.5 |
| *5* | 120 | 60 | 50, 100, 150, 250 | 0.5 |
| *7* | 120 | 60 | 50, 100, 150, 250 | 0.5 |

**Table 6.5: Experimental Set-Up for Individual Cases in *Scenario III***

*Observations:* The physical response of a circuit is unique to a given supply voltage input. Thus, different initial estimates of the load resistance $R_L$ correspond to different load levels connected to a given circuit yield. Figures 6.18 – 6.21 illustrate the way each simulated response matches the reference physical response for an input harmonic supply voltage at varying load levels. Despite the varying initial estimates, for a particular supply voltage input, the circuit parameters of the equivalent circuit converge

approximately to the same unique *Correction Factor* so that the simulated response, $I_{S,MOD}$ matches the constant reference physical response, $I_{S,\,MEAS}$.

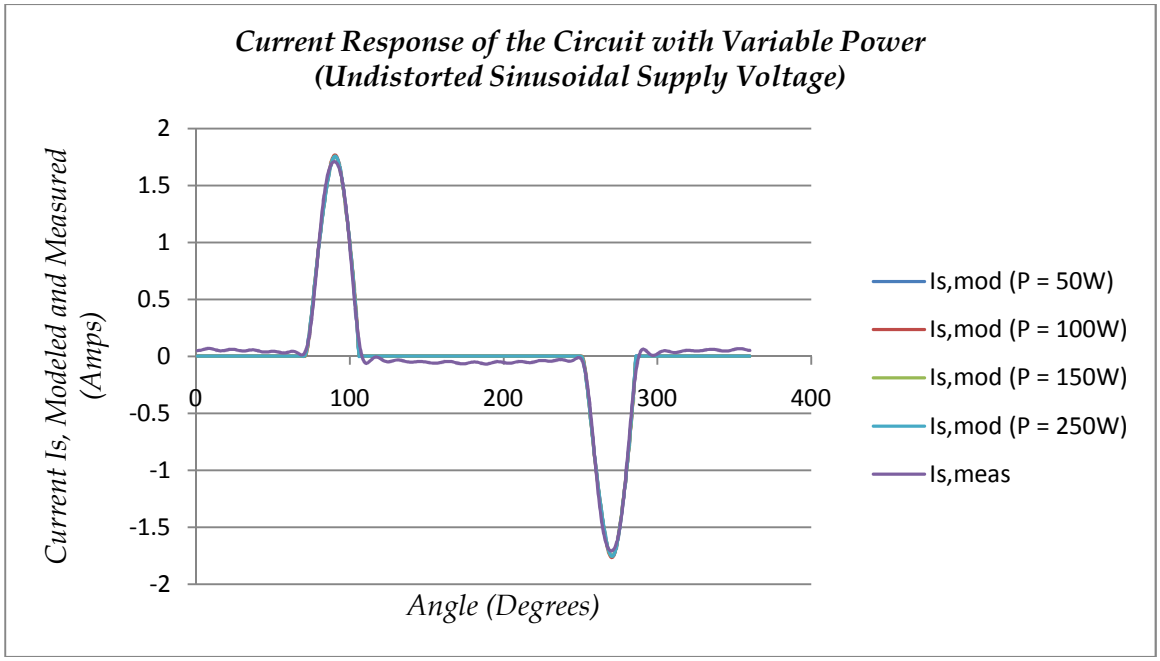



**Figure 6.18: Current Response to Varying Load $P_L$ for an Undistorted Sinusoidal Supply Voltage**

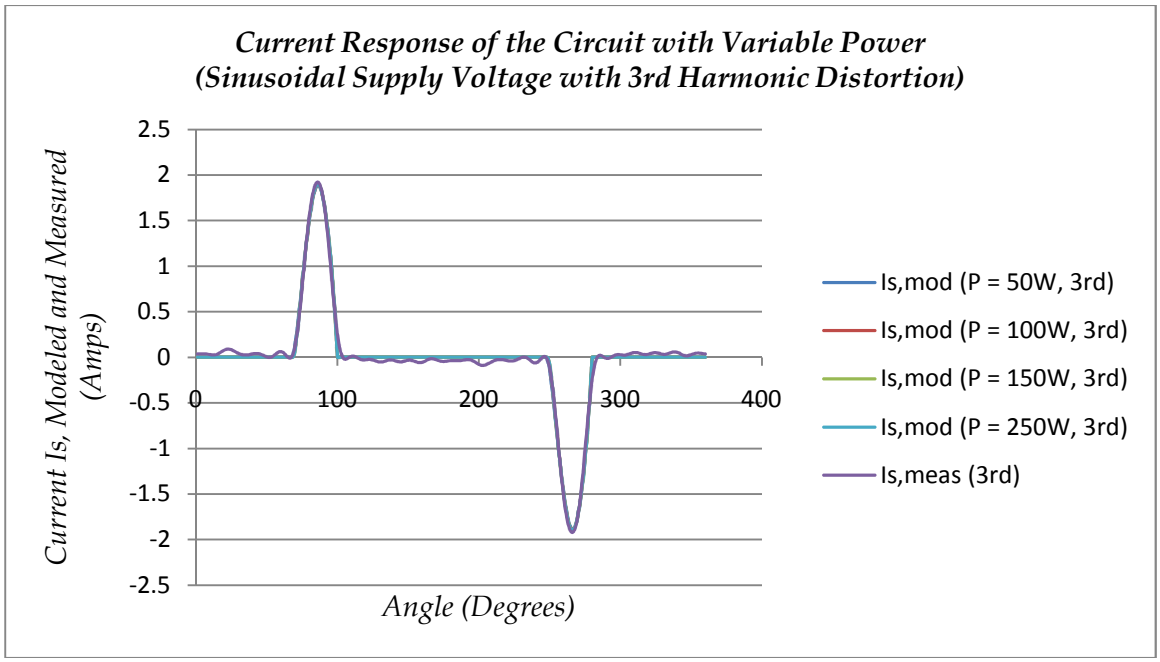



**Figure 6.19: Current Response to Varying Load $P_L$ for a Sinusoidal Supply Voltage with 3rd Harmonic Distortion Added**

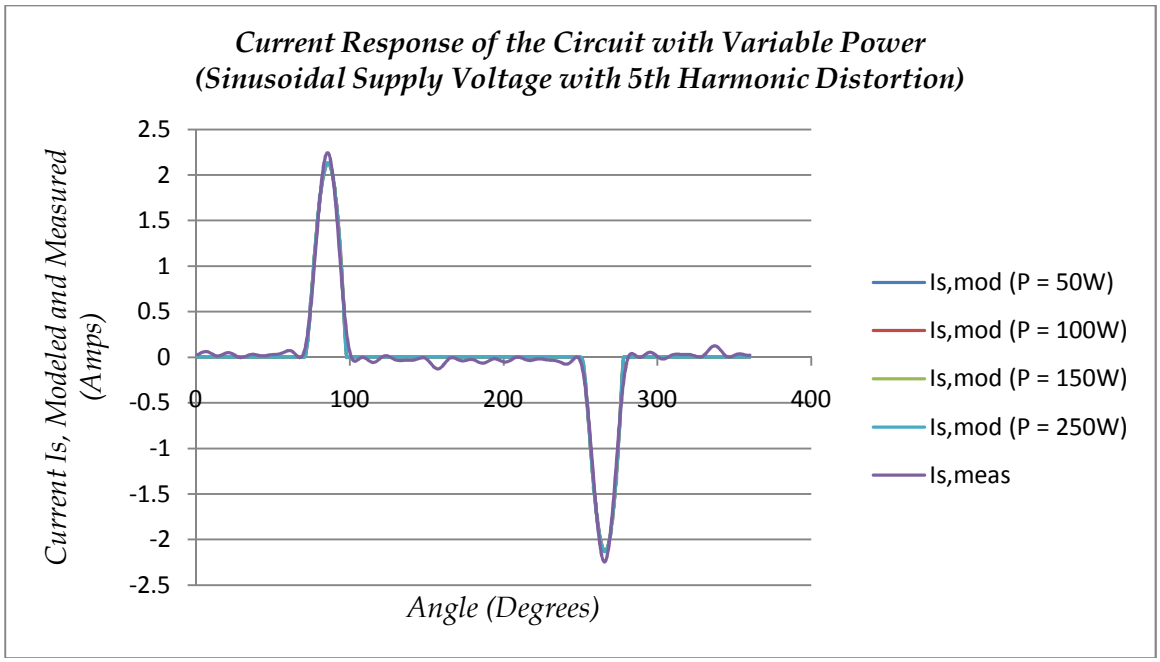



**Figure 6.20: Current Response to Varying Load $P_L$ for a Sinusoidal Supply Voltage with 5th Harmonic Distortion Added**

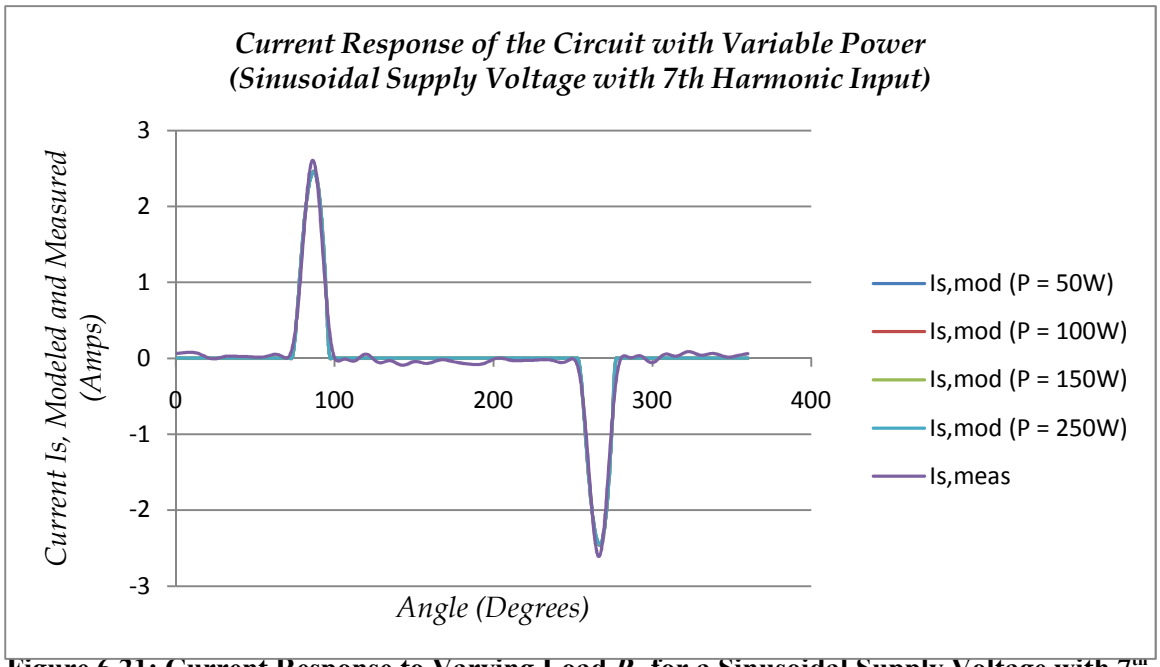



**Figure 6.21: Current Response to Varying Load $P_L$ for a Sinusoidal Supply Voltage with 7th Harmonic Distortion Added**

Hence, varying initial estimates of the resistive load caused by the variation in the load level has little impact on the optimized solution of the circuit parameters, or the *Correction Factor*. Tables 6.6 summarizes our results for each parameter at the aforementioned load levels.

| $P_L$ | $E_I$ | | C | | $R_L$ | | $R_T$ | | $L_T$ | |
|---|---|---|---|---|---|---|---|---|---|---|
| | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* |
| **1st Harmonic (Ph = 0, X/R = 0.5)** | | | | | | | | | | |
| *50* | 343.08 | 13.52 | 545.91 | 158.61 | 288.79 | 815.7 | 2.3 | 2.28 | 3.05 | 1.12 |
| *100* | 599.53 | 12.39 | 1091.81 | 196.25 | 144.4 | 807.29 | 2.3 | 2.51 | 3.05 | 0.88 |
| *150* | 809.16 | 12.75 | 1637.72 | 181.73 | 96.27 | 808.76 | 2.3 | 2.47 | 3.05 | 0.96 |
| *250* | 1144.22 | 13.56 | 2729.53 | 159.83 | 57.76 | 813.89 | 2.3 | 2.3 | 3.05 | 1.12 |
| **3rd Harmonic (Ph = 60, X/R = 0.5)** | | | | | | | | | | |
| *50* | 361.11 | 18.1 | 548.36 | 157.39 | 287.95 | 835.46 | 2.19 | 2.3 | 2.91 | 1.23 |
| *100* | 640.95 | 16.25 | 1096.71 | 240.35 | 143.98 | 844.2 | 2.19 | 2.64 | 2.91 | 0.82 |
| *150* | 862.75 | 16.06 | 1645.07 | 263.8 | 95.99 | 839.22 | 2.19 | 2.71 | 2.91 | 0.76 |
| *250* | 1221.38 | 15.94 | 2762.09 | 281.36 | 57.59 | 842.76 | 2.19 | 2.74 | 2.91 | 0.71 |
| **5th Harmonic (Ph = 60, X/R = 0.5)** | | | | | | | | | | |
| *50* | 396.75 | 20.82 | 555.49 | 158.2 | 287.76 | 860.04 | 2.07 | 2.16 | 2.75 | 1.01 |
| *100* | 688.13 | 19.74 | 1110.99 | 251.33 | 143.88 | 869.29 | 2.07 | 2.43 | 2.75 | 0.68 |
| *150* | 899.47 | 19.94 | 1666.48 | 248.73 | 95.92 | 863.99 | 2.07 | 2.47 | 2.75 | 0.69 |
| *250* | 1231.53 | 19.76 | 2777.47 | 267.15 | 57.56 | 864.62 | 2.07 | 2.46 | 2.75 | 0.64 |
| **7th Harmonic (Ph = 60, X/R = 0.5)** | | | | | | | | | | |
| *50* | 439.29 | 22.09 | 558.14 | 175.64 | 287.97 | 867.78 | 1.94 | 2.14 | 2.57 | 0.7 |
| *100* | 708.28 | 22.1 | 1116.27 | 220.91 | 143.99 | 861.39 | 1.94 | 2.42 | 2.57 | 0.6 |
| *150* | 903.24 | 21.98 | 1674.41 | 217.77 | 95.99 | 864.54 | 1.94 | 2.36 | 2.57 | 0.6 |
| *250* | 1232.51 | 21.96 | 2790.68 | 238.22 | 57.6 | 865.33 | 1.94 | 2.45 | 2.57 | 0.56 |

**Table 6.6: Optimized Solution of Circuit Parameters with Varying $P_L$ for Different Harmonic Supply Voltages**

Additionally, when different harmonic supply voltages are compared each parameter follows a similar pattern of optimization at varying load levels. Evidence for this fact is shown in Figures 6.22 – 6.26, which display the optimized solution patterns of parameters *C,* $R_L$, $R_T$ and $L_T$ respectively, in addition to the minimized error $E_I$ between the modeled and the measured current.

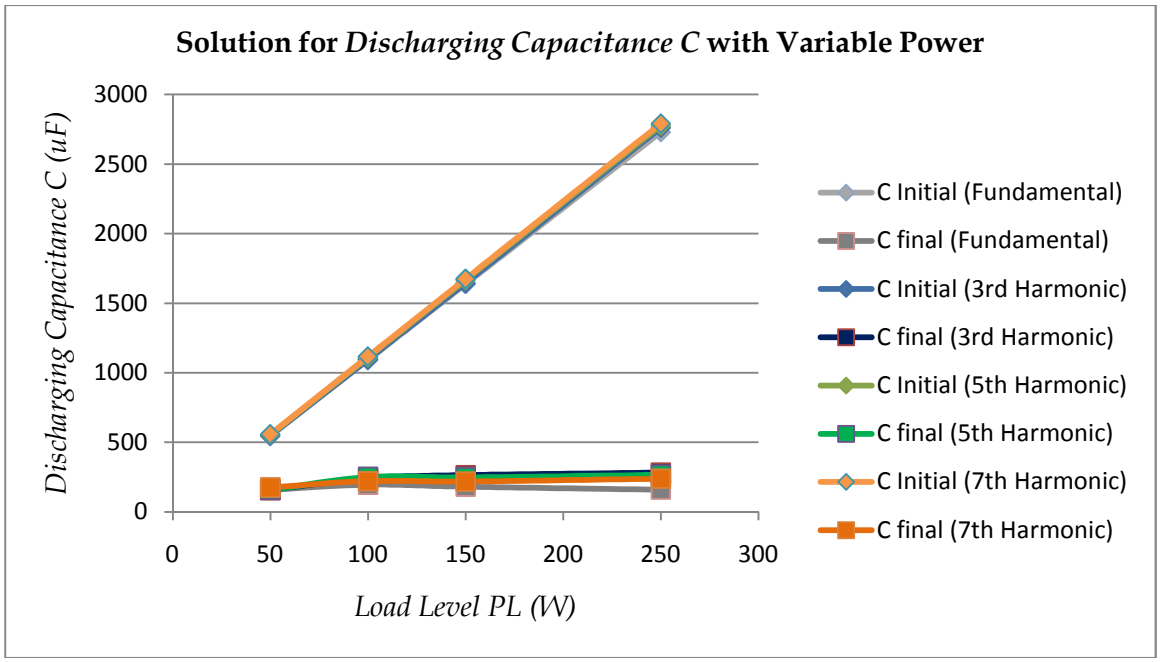



**Figure 6.22: Optimization of Discharging Capacitance C with Varying Load $P_L$ for Different Harmonic Supply Voltages**

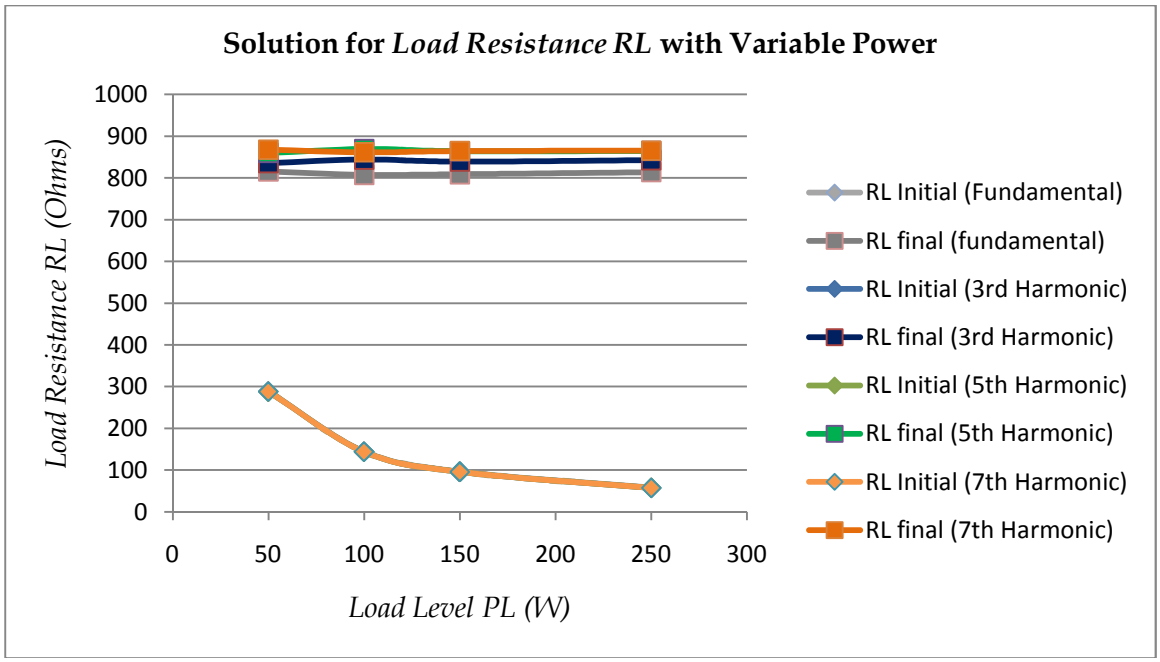



**Figure 6.23: Optimization of Load Resistance $R_L$ with Varying Load $P_L$ for Different Harmonic Supply Voltages**

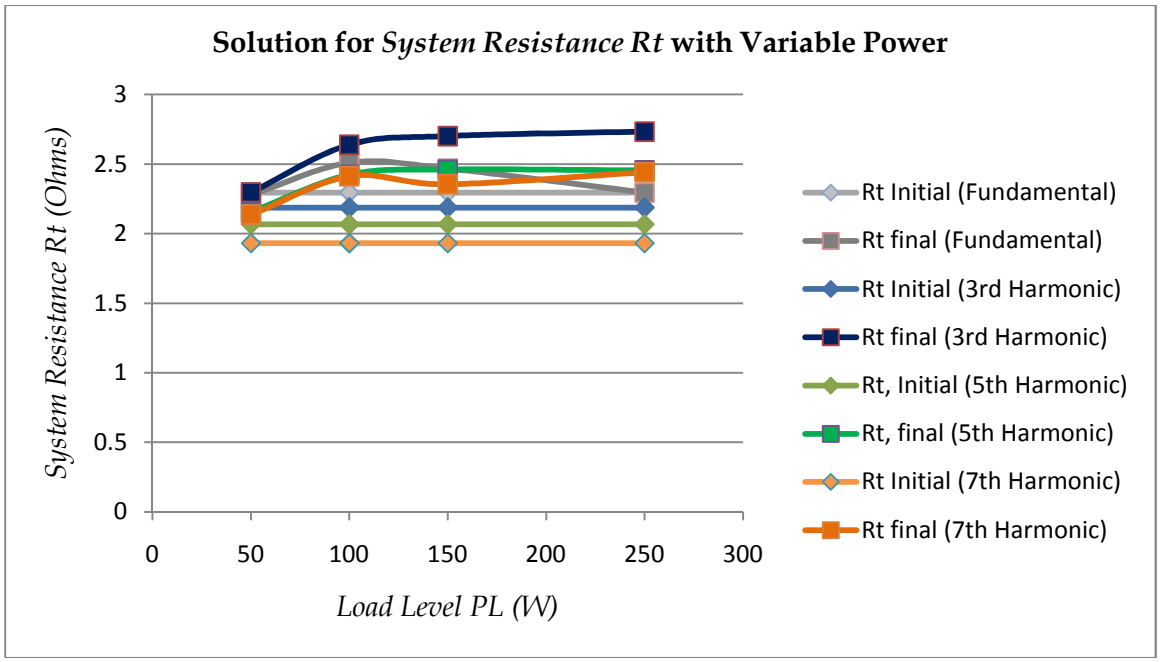



**Figure 6.24: Optimization of System Resistance $R_T$ with Varying Load $P_L$ for Different Harmonic Supply Voltages**

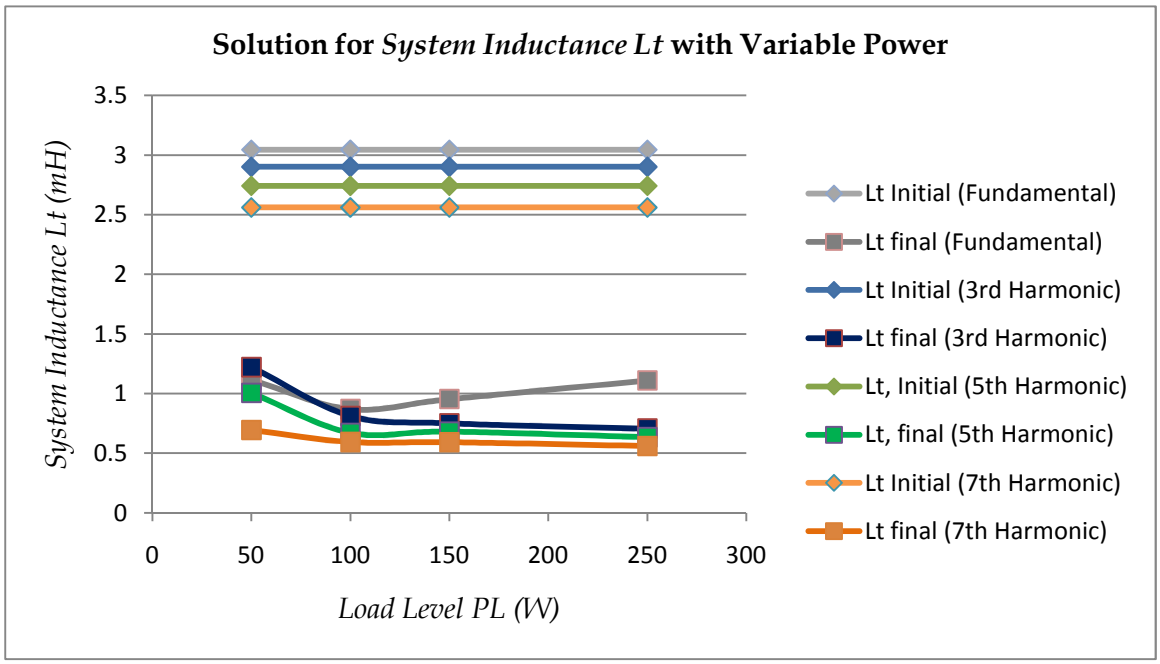



**Figure 6.25: Optimization of System Inductance $L_T$ with Varying Load $P_L$ for Different Harmonic Supply Voltages**

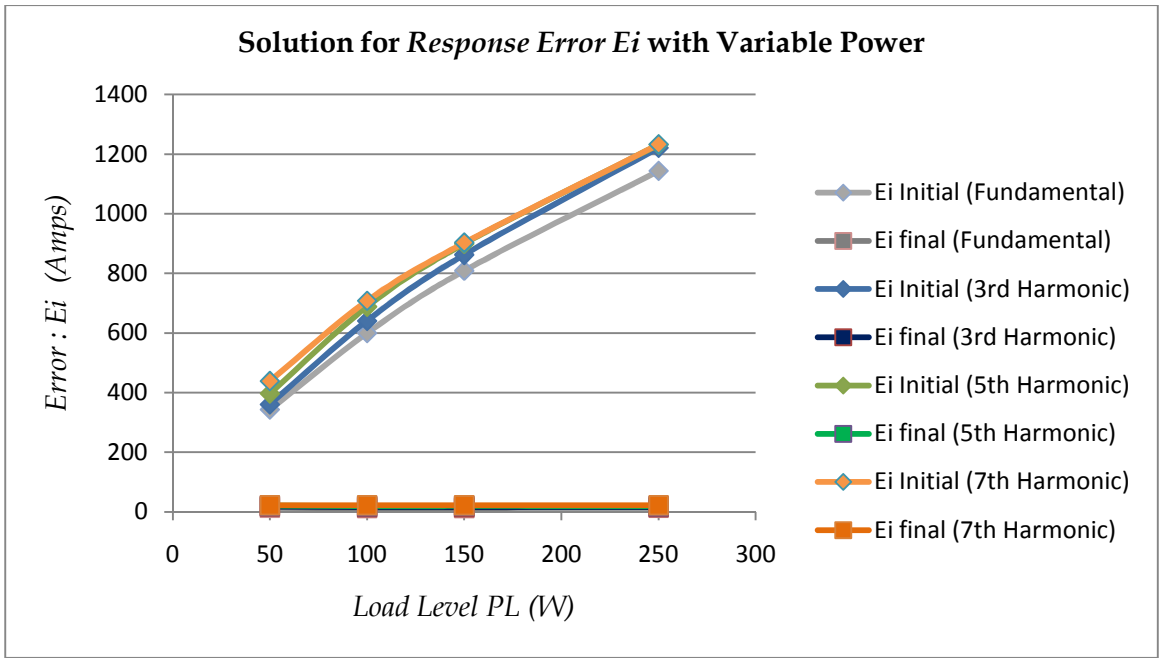



**Figure 6.26: Minimization of Current Error $E_I$ with Varying Load $P_L$ for Different Harmonic Supply Voltages**

*Conclusion:* Varying load levels, similar to the varying harmonic content of the supply voltage studied in scenario I, have little impact on the convergence of the parameters to a unique optimized solution. Despite the variable loads connected to the equivalent circuit, the parameter values always converge to generate a consistent *Correction Factor* that is unique to the given reference physical response.

## 5. SCENARIO IV: RESPONSE OPTIMIZATION WITH VARYING *X/R* RATIO OF THE EQUIVALENT CIRCUIT

*Scenario Description:* The given scenario analyses the effect of varying the *X/R* ratio on the simulated response of the equivalent circuit. *X/R* is defined as the ratio of system reactance, $X_T = j\omega L_T$ to system resistance, $R_T$. The *X/R* ratio is used to determine the initial estimates for $R_T$ and $X_T$. Mathematically, this relationship is expressed as:

$$R_T(\Omega) = V_{IN,fundamental} \times \frac{(1-0.98)}{I_{des,rms}} \ldots (2)$$

$$L_T(mH) = \left(\frac{X}{R}\right) \times \frac{R_T}{(120 \times PI)} \ldots (3)$$

$Where-$ 0.98 is based on the assumption that $V_{OUT}$ = 98% of $V_{IN}$ and

$V_T = V_{IN} - V_{OUT}$

A 120 Vrms sinusoidal input powered the equivalent circuit model to which the 3rd, 5th and 7th harmonics were subsequently and separately added. During the simulation, the phase-shift for each supply voltage input was maintained at 165°, except the fundamental signal. It was simulated without any phase-shift. For each supply voltage input, we simulate the circuit, with variable *X/R* ratios and a constant load $P_L$ = 100 W connected to it. The experiment's constraints for Scenario IV are recorded in Table 6.7.

| | Vrms | | | |
|---|---|---|---|---|
| **Harmonic #** | **Magnitude (V)** | **Phase (°)** | **$P_L$ (Watts)** | **X/R** |
| *1* | 120 | 0 | 100 | 0.2, 0.5, 0.75, 1.0, 2.0, 5.0 |
| *3* | 120 | 165 | 100 | 0.2, 0.5, 0.75, 1.0, 2.0, 5.0 |
| *5* | 120 | 165 | 100 | 0.2, 0.5, 0.75, 1.0, 2.0, 5.0 |
| *7* | 120 | 165 | 100 | 0.2, 0.5, 0.75, 1.0, 2.0, 5.0 |

**Table 6.7: Experimental Set-Up for Individual Cases in *Scenario IV***

*Observations:* For a constant system resistance, $R_T$, variable *X/R* ratio generates variable values for the system inductance, $L_T$. Figures 6.27 – 6.30 illustrate the accuracy of the match of the simulated response to the physical response corresponding to the variation in the *X/R* ratio for different harmonic supply voltages.

Theoretically, the simulated circuit response should match the physical response, as the circuit parameters converge to a unique, consistent, optimized solution, notwithstanding their initial estimates. In each case that the simulated response follows this hypothesis for X/R ratios less than and equal to 1.0, the optimized parameter values will converge within a narrow range though each parameter appears to a follows an idiosyncratic pattern. Discharging capacitance $C$ and system resistance $R_T$ decrease with the increasing $X/R$ ratio for each harmonic supply voltage input, while the system inductance $L_T$ increases. Load resistance $R_L$ is not very sensitive to $X/R$ variation; remaining essentially constant for the entire $X/R$ spectrum. We note a certain loss of accuracy and divergence in the optimized results for $X/R$ ratios 2 and 5. This is indicative of the fact that a realistic $X/R$ ratio for the given load level is less than 1.

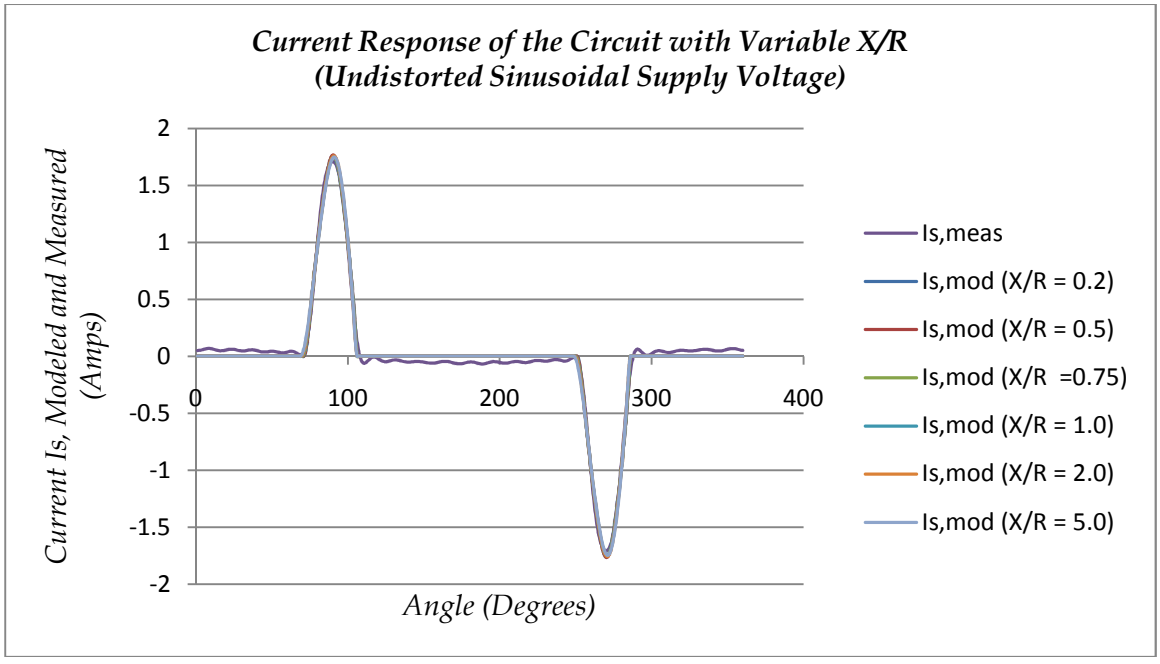



**Figure 6.27: Current Response to Varying *X/R* for an Undistorted Sinusoidal Supply Voltage**

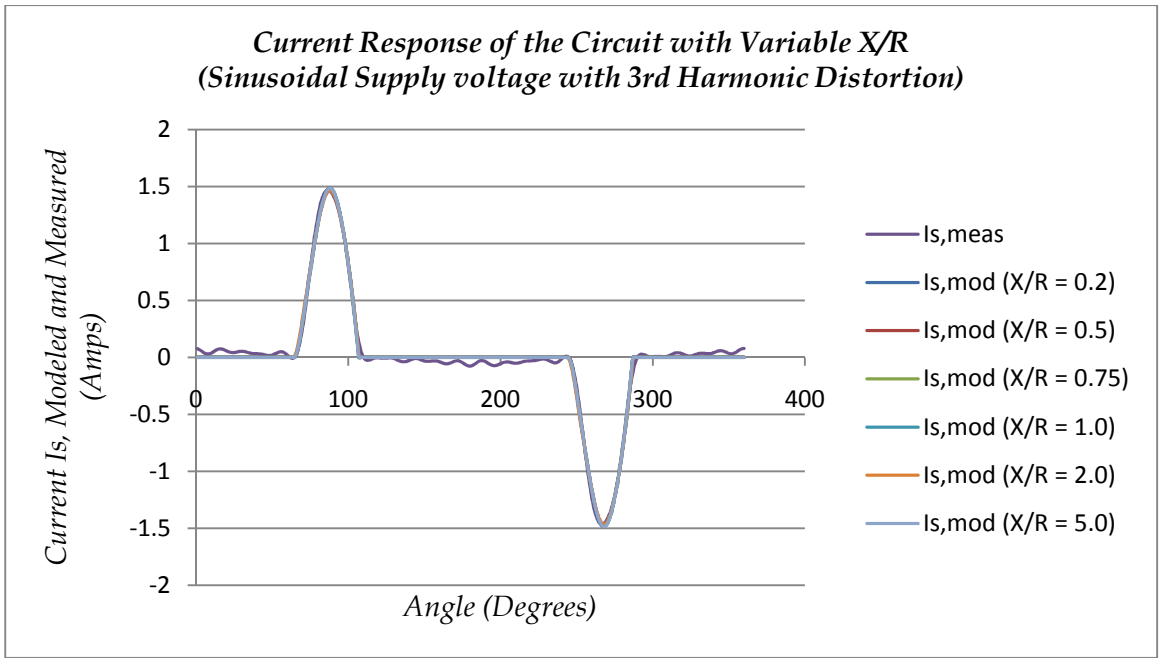



**Figure 6.28: Current Response to Varying *X/R* for an Sinusoidal Supply Voltage with 3rd Harmonic Distortion Added**

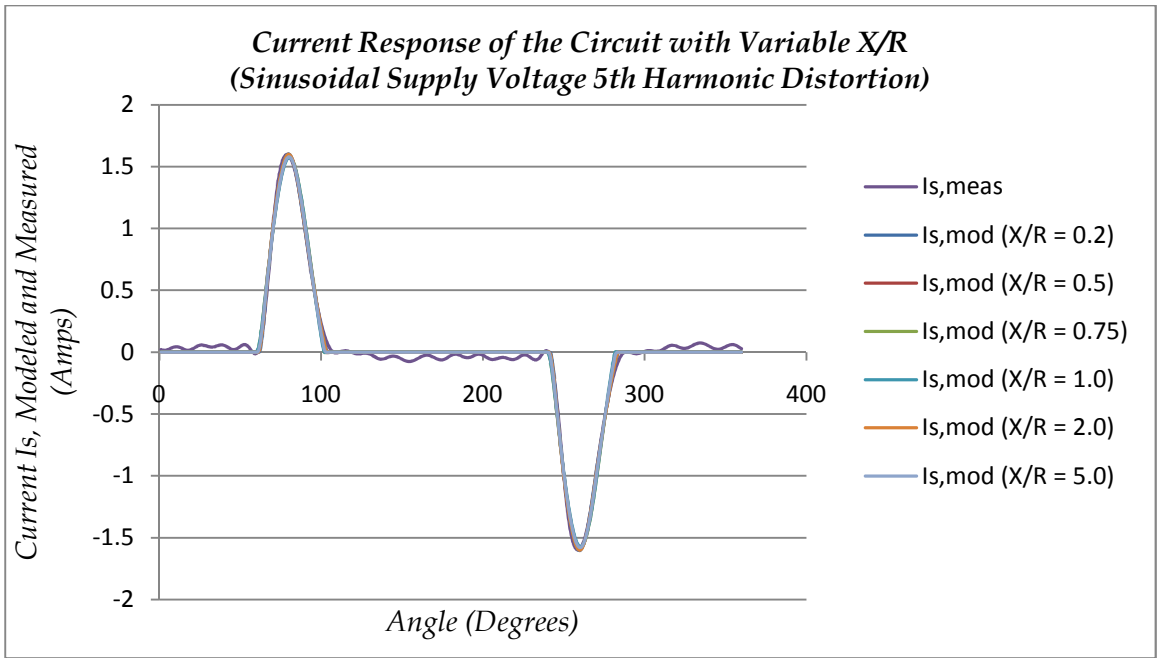



**Figure 6.29: Current Response to Varying *X/R* for a Sinusoidal Supply Voltage with 5th Harmonic Distortion Added**

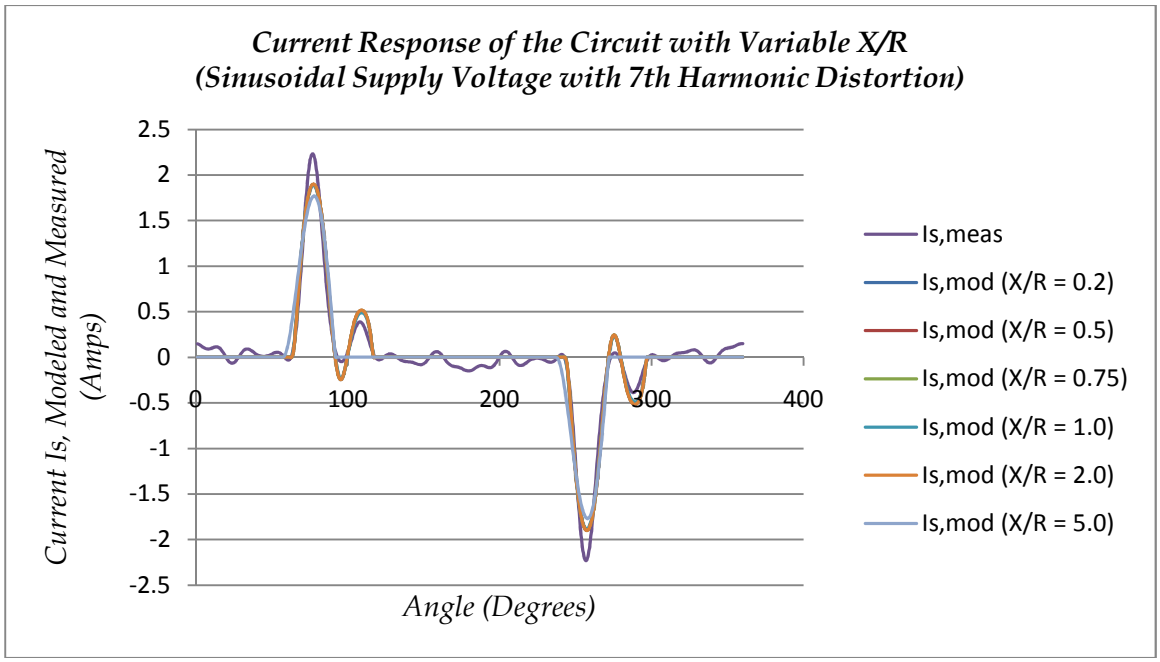



**Figure 6.30: Current Response to Varying *X/R* for a Sinusoidal Supply Voltage with 7th Harmonic Distortion Added**

Tables 6.8 summarizes the Scenario IV results. Figures 6.31 – 6.35 display optimized parameter solutions, also known as the correction factor and the minimized error computed for the equivalent circuit with varying *X/R*.

| 1st Harmonic (Ph = 0, PL = 100W) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| X/R | $E_I$ | | C | | $R_L$ | | $R_T$ | | $L_T$ | |
| | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* |
| *0.2* | 519.8 | 12.88 | 1094.51 | 172.6 | 144.4 | 815.36 | 4.6 | 2.39 | 2.44 | 1.02 |
| *0.5* | 496.47 | 15.86 | 1094.51 | 129.46 | 144.4 | 815.12 | 4.6 | 2.05 | 6.1 | 1.44 |
| *0.75* | 477.63 | 16.08 | 1094.51 | 129.91 | 144.4 | 809.62 | 4.6 | 2.06 | 9.14 | 1.45 |
| *1* | 455.83 | 18.32 | 1094.51 | 92.02 | 144.4 | 816.82 | 4.6 | 1.09 | 12.19 | 2.05 |
| *2* | 432.58 | 17.45 | 1094.51 | 100.77 | 144.4 | 816.65 | 4.6 | 1.34 | 18.28 | 1.84 |
| *5* | 413.83 | 17.9 | 1094.51 | 97.47 | 144.4 | 814.06 | 4.6 | 1.29 | 24.37 | 1.94 |
| **3rd Harmonic (Ph = 165, PL =100W)** | | | | | | | | | | |
| *0.2* | 530.29 | 13.86 | 1068.79 | 265.77 | 143.82 | 757.51 | 4.92 | 2.74 | 2.61 | 0.98 |
| *0.5* | 499.51 | 14.67 | 1068.79 | 216.24 | 143.82 | 764.85 | 4.92 | 2.52 | 6.53 | 1.22 |
| *0.75* | 475.04 | 15.07 | 1068.79 | 200.32 | 143.82 | 767.44 | 4.92 | 2.43 | 9.79 | 1.32 |
| *1* | 465.51 | 15.17 | 1068.79 | 199.69 | 143.82 | 761.15 | 4.92 | 2.47 | 13.05 | 1.34 |
| *2* | 418.56 | 17.15 | 1068.79 | 180.33 | 143.82 | 760.54 | 4.92 | 2.52 | 26.1 | 1.52 |
| *5* | 308.67 | 15.72 | 1070.82 | 186.22 | 143.82 | 758.74 | 4.92 | 2.41 | 65.25 | 1.45 |
| **5th Harmonic (Ph = 165, PL =100W)** | | | | | | | | | | |
| *0.2* | 423.29 | 20.94 | 1065.14 | 253.17 | 143.3 | 754.8 | 4.75 | 3.2 | 2.52 | 1.03 |
| *0.5* | 436.62 | 22.28 | 1065.14 | 221.68 | 143.3 | 762.27 | 4.75 | 3.15 | 6.3 | 1.19 |
| *0.75* | 435.06 | 25.32 | 1065.14 | 173.61 | 143.3 | 756.83 | 4.75 | 3.2 | 9.44 | 1.56 |
| *1* | 419.98 | 25.79 | 1065.14 | 170.52 | 143.3 | 756.67 | 4.75 | 3.26 | 12.59 | 1.6 |
| *2* | 391.09 | 19.75 | 1065.14 | 280.02 | 143.3 | 760.89 | 4.75 | 3.18 | 25.17 | 0.92 |
| *5* | 337.5 | 19.91 | 1065.14 | 276.95 | 143.3 | 766.11 | 4.75 | 3.14 | 62.91 | 0.93 |
| **7th Harmonic (Ph = 165, PL =100W)** | | | | | | | | | | |
| *0.2* | 559.03 | 54.15 | 1110.42 | 449.31 | 144.26 | 773.8 | 4.31 | 3.69 | 2.29 | 0.51 |
| *0.5* | 520.56 | 54.15 | 1113.46 | 448.18 | 144.26 | 773.8 | 4.31 | 3.7 | 5.71 | 0.51 |
| *0.75* | 516.53 | 54.14 | 1113.46 | 447.78 | 144.26 | 773.97 | 4.31 | 3.69 | 8.57 | 0.51 |
| *1* | 503.81 | 54.12 | 1113.46 | 465.65 | 144.26 | 777.69 | 4.31 | 3.67 | 11.42 | 0.5 |
| *2* | 476.25 | 54.14 | 1113.46 | 451.07 | 144.26 | 777.22 | 4.31 | 3.68 | 22.84 | 0.51 |
| *5* | 407.05 | 88.4 | 1113.46 | 32.44 | 144.26 | 847.72 | 4.31 | 0.18 | 57.1 | 5.62 |

**Table 6.8: Optimized Solution of the Circuit Parameters with Varying *X/R* for Different Harmonic Supply Voltages**

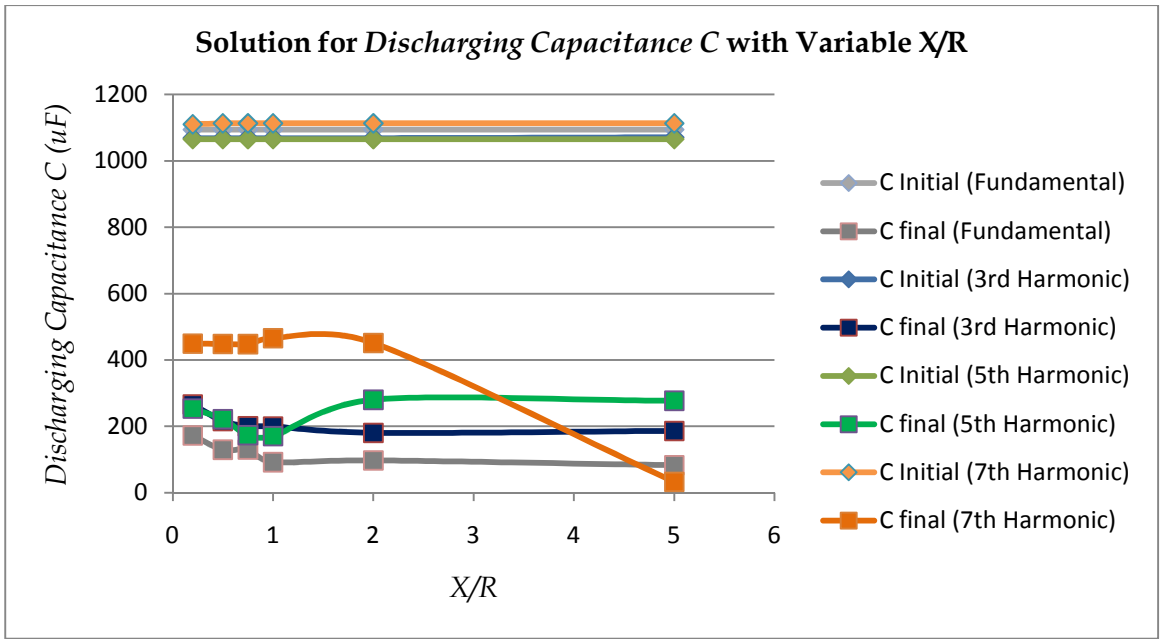



**Figure 6.31: Optimization of Discharging Capacitance C with Varying *X/R* for Different Harmonic Supply Voltages**

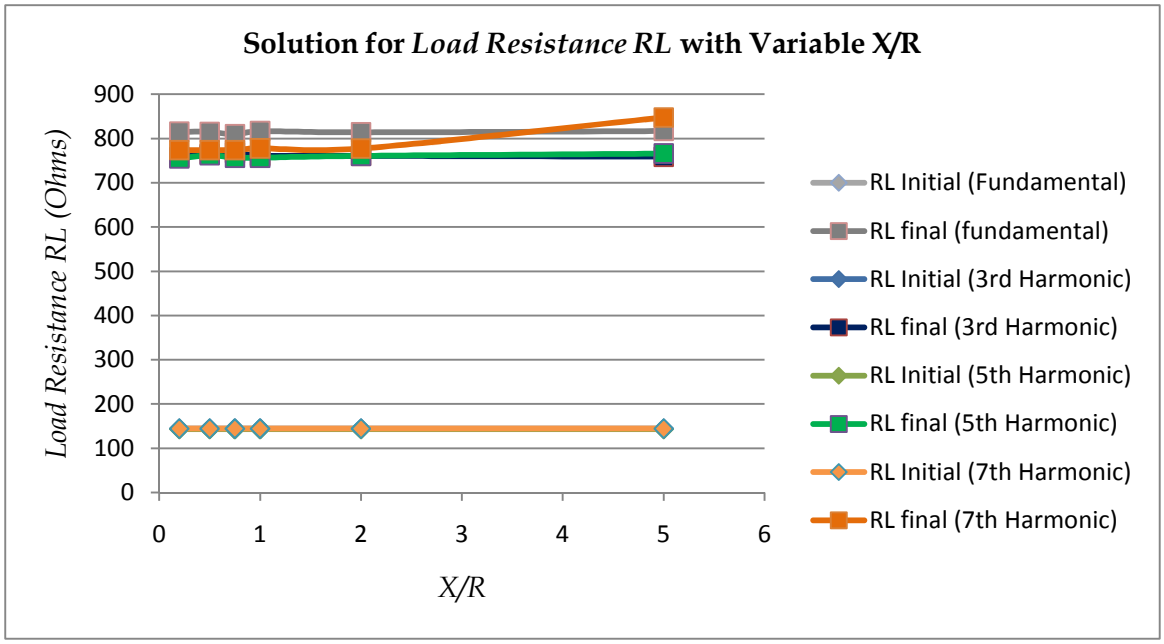



**Figure 6.32: Optimization of Load Resistance $R_L$ with Varying *X/R* for Different Harmonic Supply Voltages**

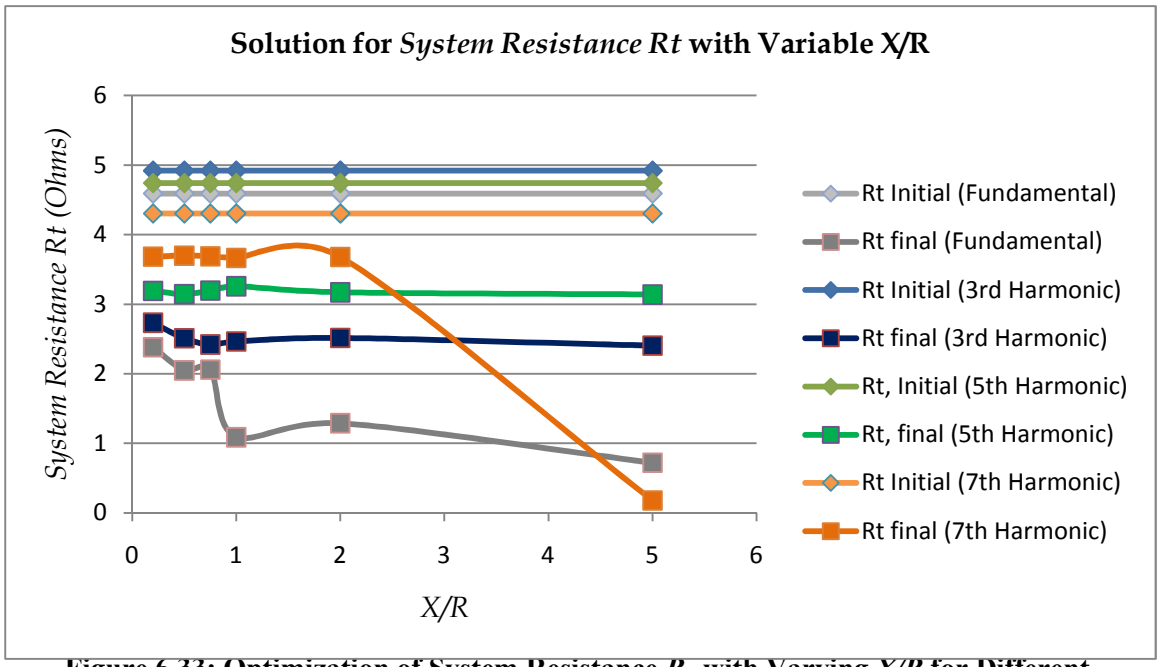



**Figure 6.33: Optimization of System Resistance $R_T$ with Varying *X/R* for Different Harmonic Supply Voltages**

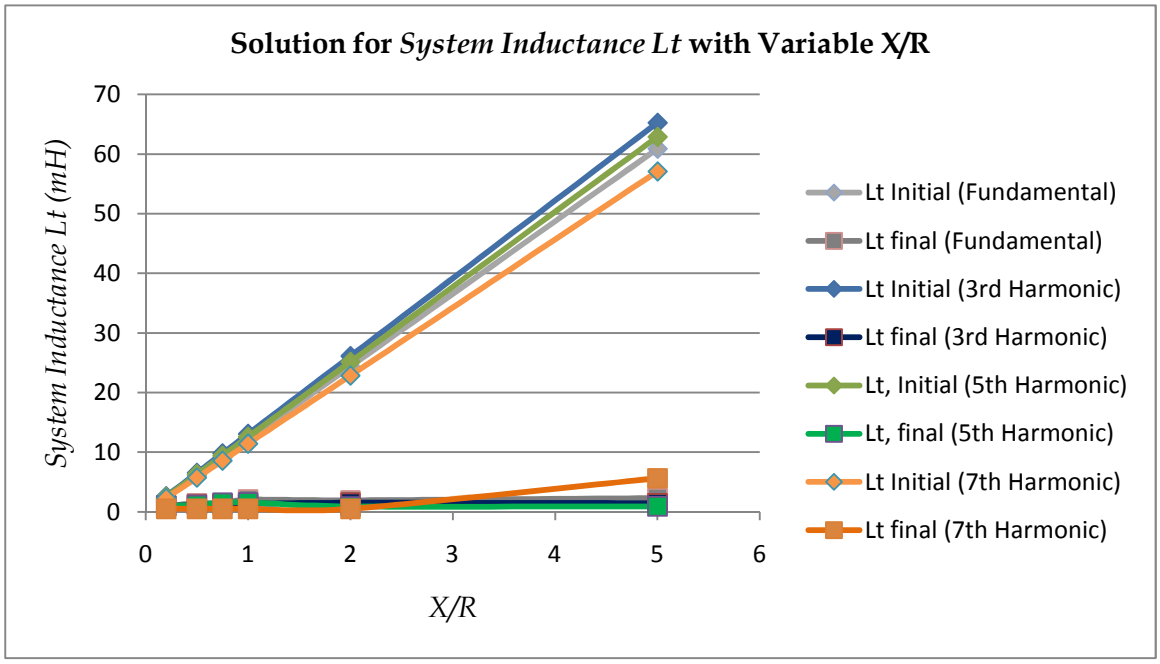



**Figure 6.34: Optimization of System Inductance $L_T$ with Varying *X/R* for Different Harmonic Supply Voltages**

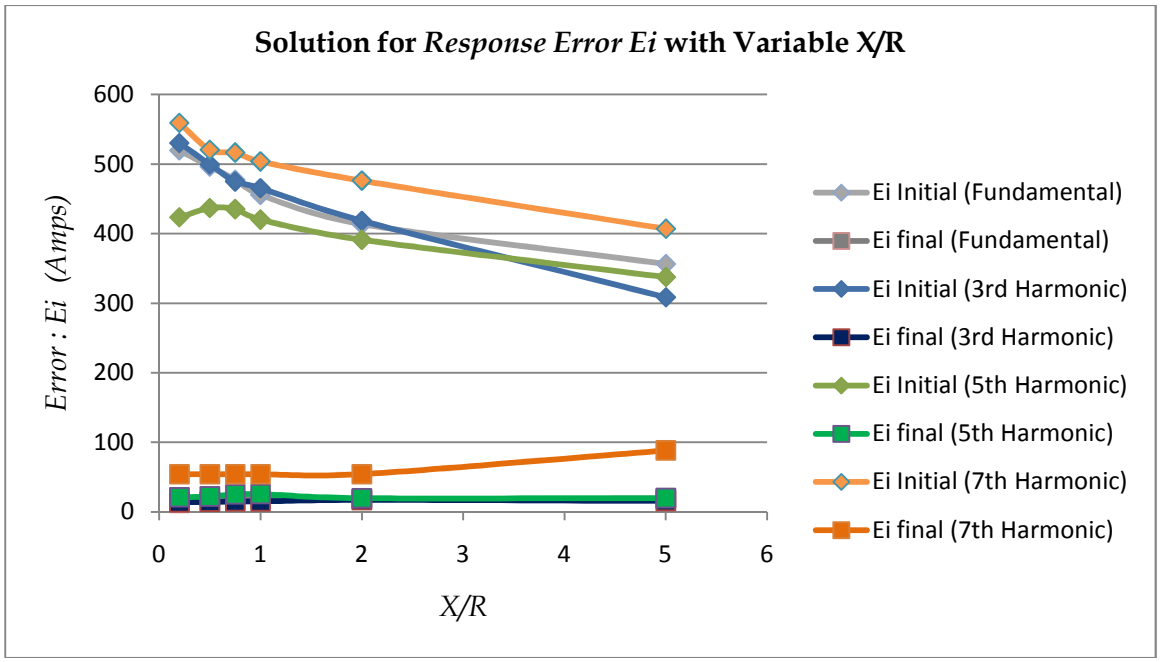



**Figure 6.35: Minimization of Current Error $E_I$ with Varying *X/R* for Different Harmonic Supply Voltages**

*Conclusion:* For a given harmonic supply voltage input, the parameters converge to a common optimized solution for an X/R less than or equal to 1.0. Each parameter however tends to follow a certain pattern that indicates its sensitivity to the X/R variation. The following patterns were observed:

- Capacitance $C$ decreases with increasing *X/R* ratio
- Load Resistance $R_L$ remains constant for variable *X/R* ratio
- System Resistance $R_T$ remains constant for variable *X/R* ratio.
- System Inductance $L_T$ increases with increasing *X/R* ratio

Loss of accuracy in the optimization of the *Correction Factor* was observed for X/R ratios, 2 and 5. This is indicative of the fact that a realistic solution of parameters exists within an X/R < 1.

## 6. SCENARIO V: SPECIAL CASES

*Scenario Description:* Certain special cases have been identified by the uniqueness of their circuit response which is reflected by the shape of their input current pulse, $I_{S,\,MEAS}$. These responses were observed, especially, with the $7^{th}$ and the $5^{th}$ harmonics, separately added to the input supply voltage with varying phases.

*Case I:* We add the $7^{th}$ harmonic to the supply voltage with approximately 5% distortion and a phase-shift varying between 150° – 210°. X/R ratio was maintained at 0.75. Table 6.9 summarizes these results.

Figures 6.36 – 6.40 display the unique shape of the input current pulse for each case listed above. These Figures trace the dual-humped current pulse with phase variation in the input supply voltage. The beginnings of a second hump are observed at phase-shift = 150°; it gains more prominence with the increase in the phase-shift angle while the first hump begins to disappear through phase-shift = 210°. Figure 6.41 records the collective progression of measured physical current pulse for phase shifts ranging from 150° – 210°.

| **7th Harmonic (X/R = 0.75, PL =100W)** | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Phase** | **$E_I$** | | **C** | | **$R_L$** | | **$R_T$** | | **$L_T$** | |
| **+** | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* |
| *150* | 533.89 | 70.47 | 1067.21 | 149.32 | 144.07 | 743.25 | 3.93 | 5.53 | 7.81 | 1.58 |
| *165* | 516.53 | 54.14 | 1113.46 | 447.78 | 144.26 | 773.97 | 4.31 | 3.69 | 8.57 | 0.51 |
| *180* | 451.45 | 22.28 | 926.68 | 549.11 | 143.89 | 820.44 | 5.41 | 3.16 | 10.75 | 0.38 |
| *195* | 452.31 | 30.59 | 989.99 | 631.54 | 144.34 | 826.82 | 5.14 | 3.1 | 10.22 | 0.36 |
| *210* | 474.07 | 25.77 | 1107.01 | 206.47 | 144.35 | 833.48 | 4.34 | 2.01 | 8.63 | 0.67 |

**Table 6.9: Optimized Solution of the Circuit Parameters with Varying *Phase Shift* for a Sinusoidal Supply Voltage with $7^{th}$ Harmonic Distortion Added**

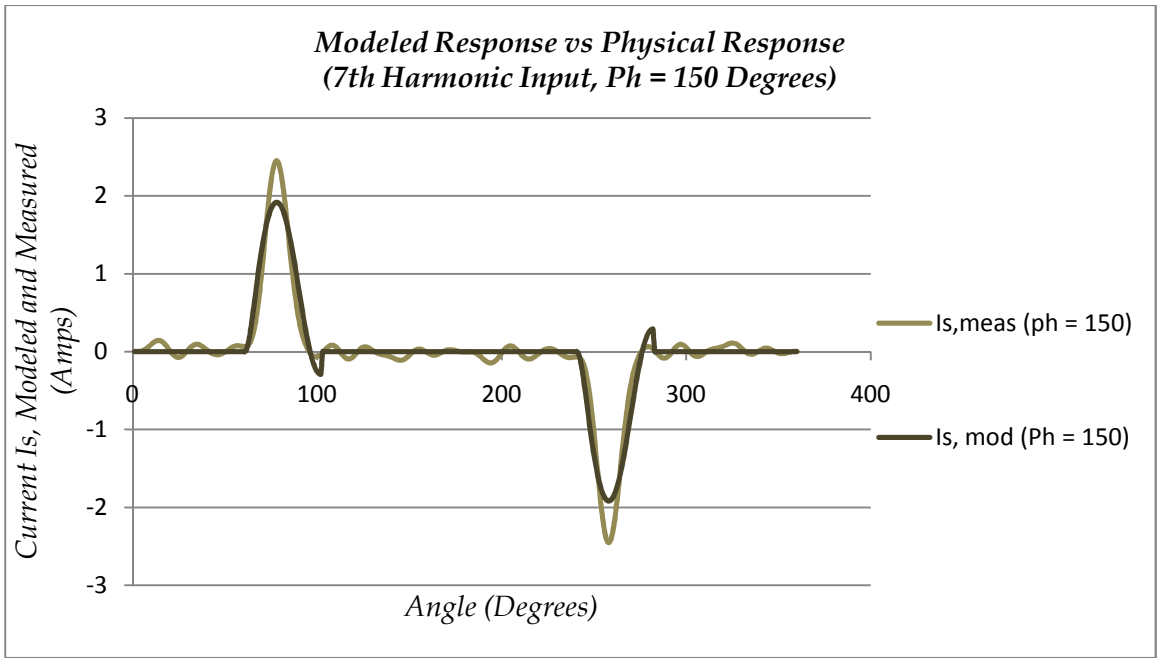



**Figure 6.36: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 7th Harmonic Distortion and Phase Shift = 150°**

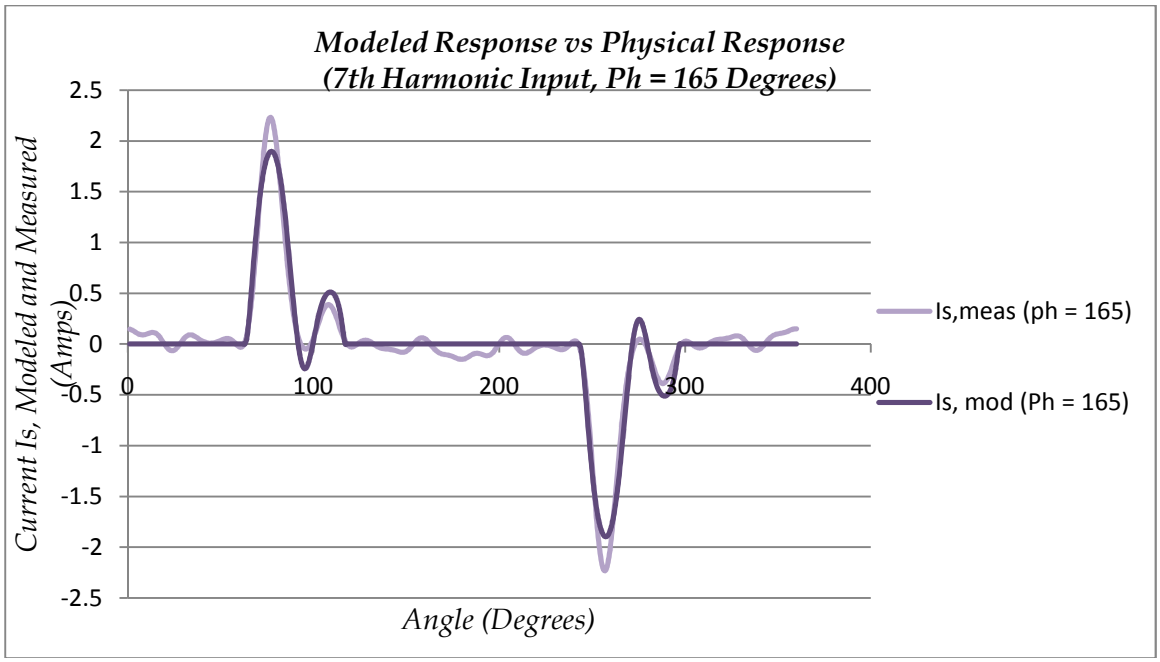



**Figure 6.37: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 7th Harmonic Distortion and Phase Shift = 165°**

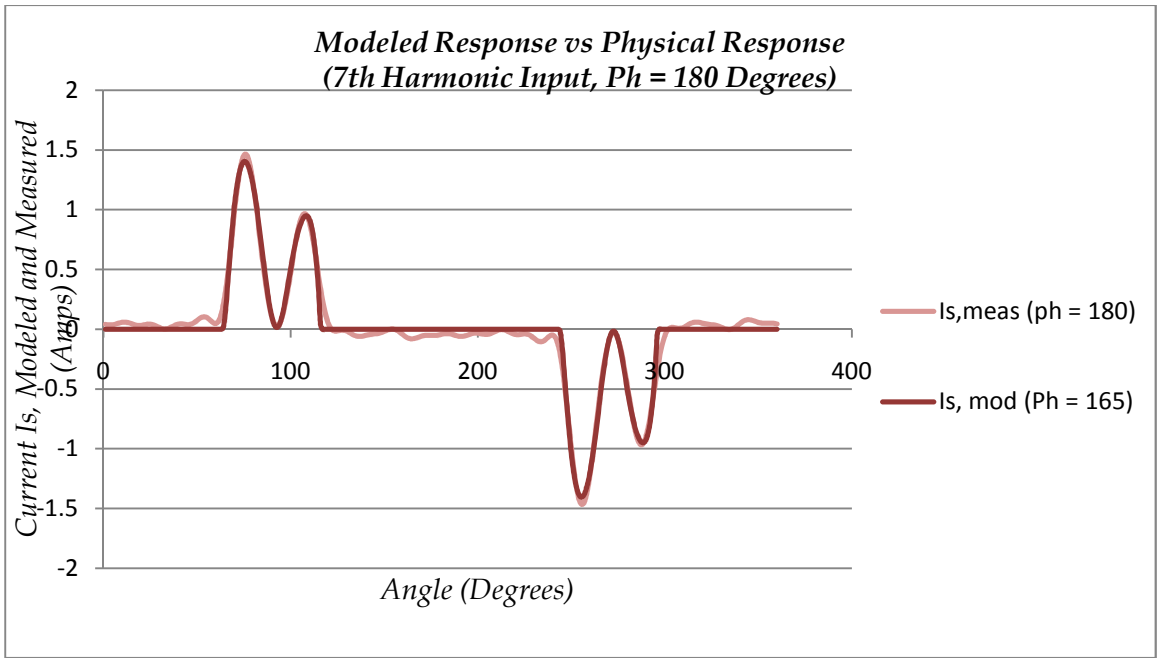



**Figure 6.38: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 7th Harmonic Distortion and Phase Shift = 180°**

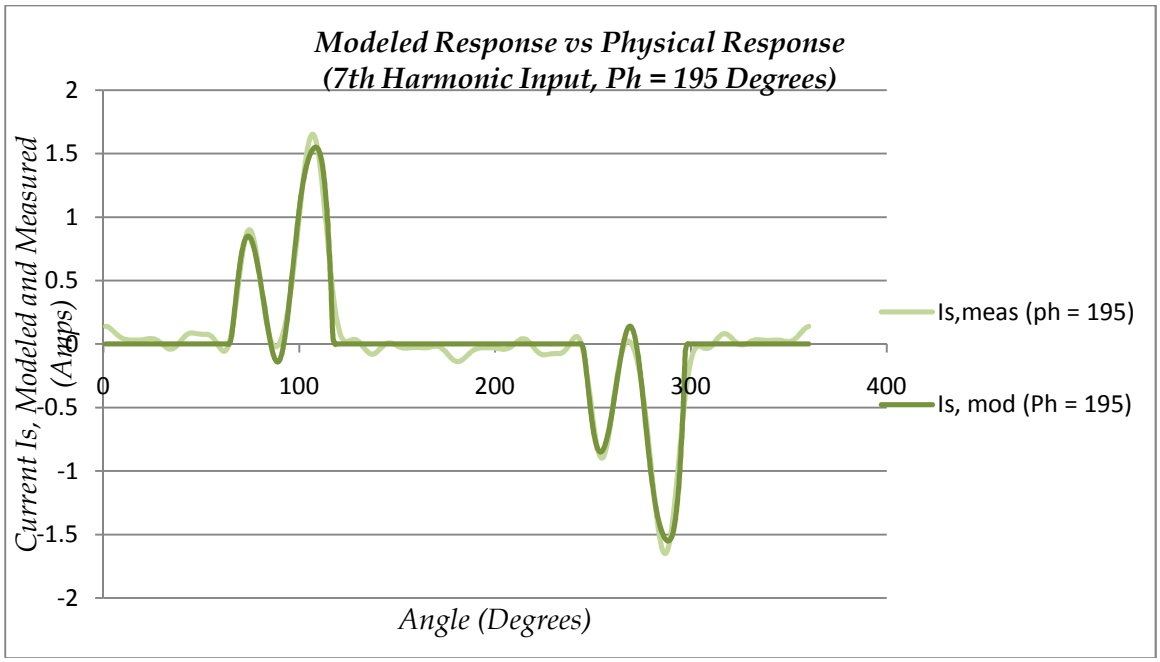



**Figure 6.39: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 7th Harmonic Distortion and Phase Shift = 195°**

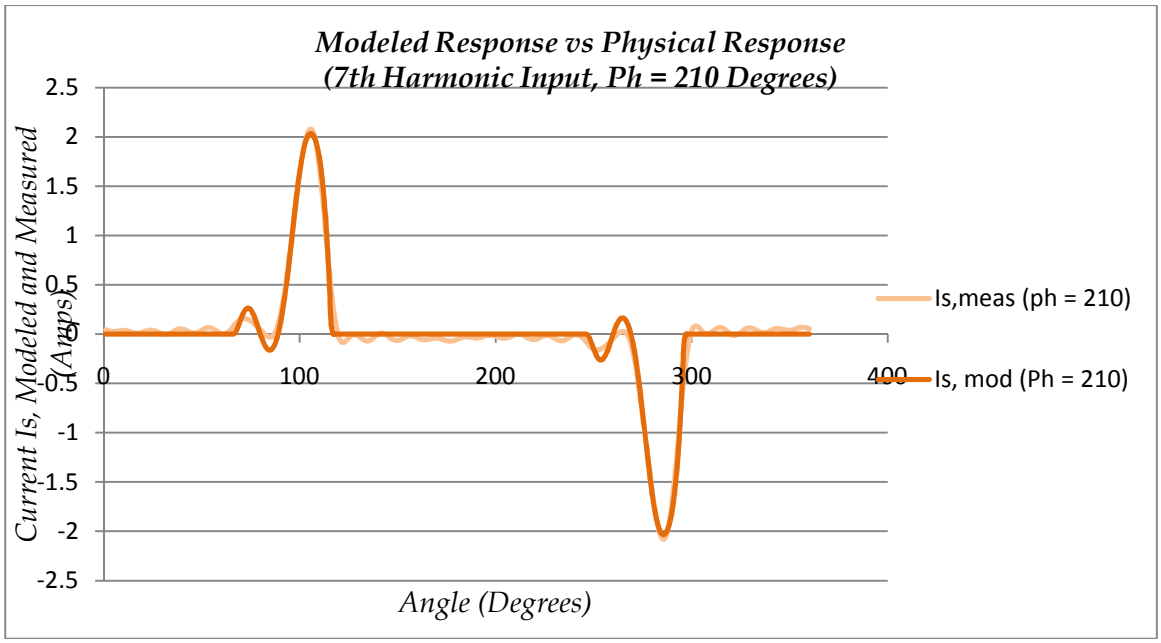



**Figure 6.40: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 7th Harmonic Distortion and Phase Shift = 210°**

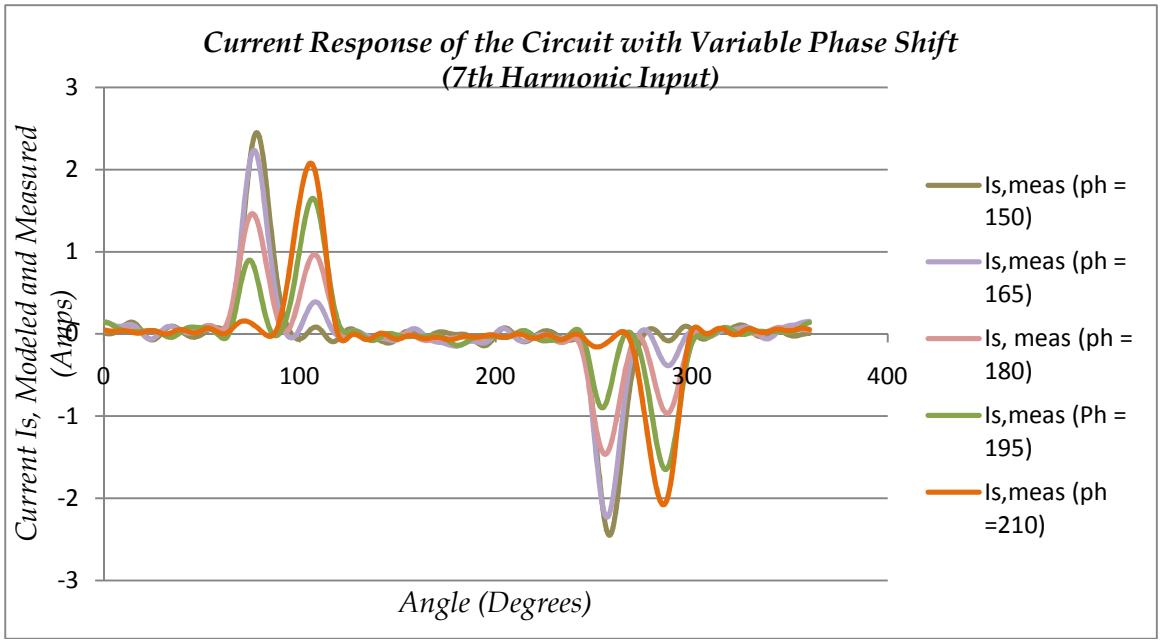



**Figure 6.41: Collective Physical Response $I_{S,MEAS}$ to Varying Phase-Shift = 150° - 210° for an Input Sinusoidal Supply Voltage with 7th Harmonic Distortion Added**

Among the cases listed above are some, in which the optimization algorithm does not correct $I_{S,\ MOD}$, the modeled response, to the desired physical response, $I_{S,\ MEAS}$. In these cases, the circuit elements do not converge to an optimized *Correction Factor*. The parameters in all these cases, with the exception of the one with phase-shift = 180°, do not converge within a desired margin of error.

We are thus tasked weith the problem of manually correcting the parameters to achieve an accurate modeled response. Parameters, $C$, $R_L$, $R_T$ and $L_T$, are incremented one at a time, or some subset of them is corrected simultaneously, to reduce the difference between the modeled and the physical response of the equivalent circuit. An appropriate parameter-increment value is added to (or subtracted from) the circuit element being corrected manually. We can enter this parameter increment directly, or calculate it as a percentage of the existing value of the circuit element.

*Case II:* A similar analysis was conducted for the $5^{th}$ harmonic added to the supply voltage with a phase angle variation from 120°, 165° – 210°. The results, summarized in Table 6.10. Figures 6.42 – 6.46, illustrate the effect of the phase-shift variation on the input supply current. Figure 6.47 displays the progression of the measured physical input current pulse with the phase-shift.

| 5th Harmonic (X/R = 0.75, PL =100W) | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Phase** | **$E_I$** | | **C** | | **$R_L$** | | **$R_T$** | | **$L_T$** | |
| **+** | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* | *Initial* | *Final* |
| *120* | 491.38 | 48.59 | 1086.29 | 146.77 | 144.15 | 797.74 | 4.24 | 3.11 | 8.43 | 1.33 |
| *165* | 435.27 | 37.8 | 1079.77 | 120.59 | 143.3 | 727.37 | 4.75 | 4.5 | 9.44 | 2.71 |
| *180* | 386.07 | 26.69 | 1036.81 | 108.39 | 143.18 | 764.02 | 5.87 | 4.12 | 11.68 | 4.97 |
| *195* | 390.1 | 23.05 | 1037.82 | 281.05 | 144.3 | 769.82 | 5.58 | 2.18 | 11.1 | 1.23 |
| *210* | 429.06 | 74.3 | 1079.41 | 154.33 | 143.89 | 745.04 | 4.71 | 3.64 | 9.37 | 2.91 |

**Table 6.10: Optimized Solution of the Circuit Parameters with Varying Phase Shift for a Sinusoidal Supply Voltage with 5th Harmonic Distortion Added**

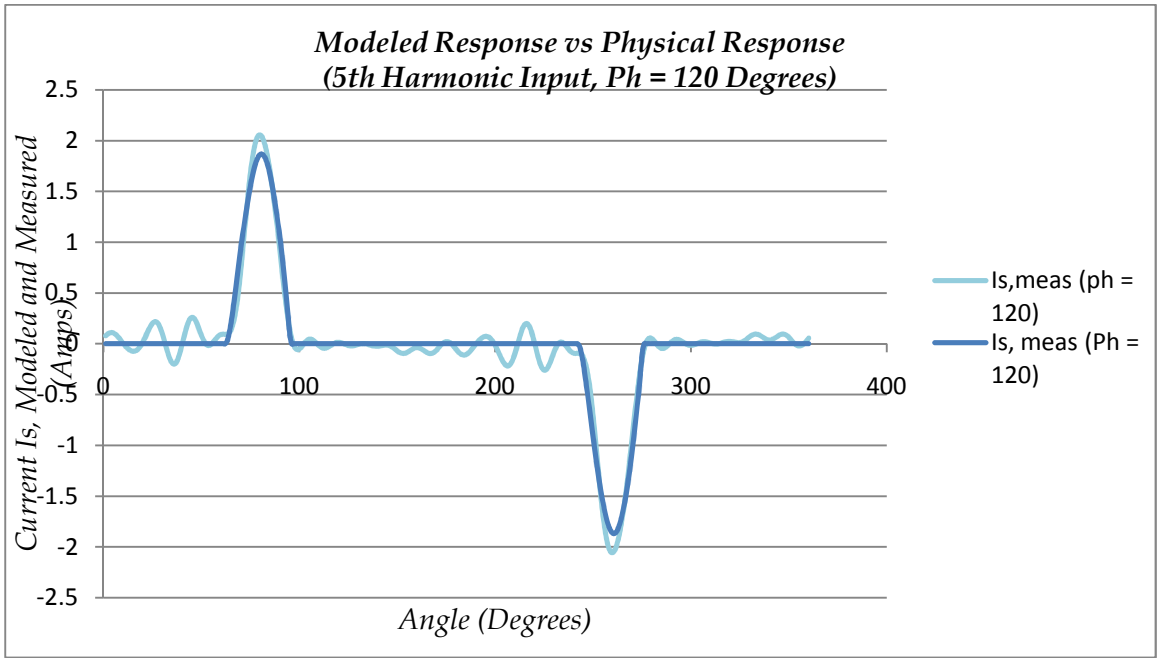



**Figure 6.42: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 5th Harmonic Distortion and Phase Shift = 120°**

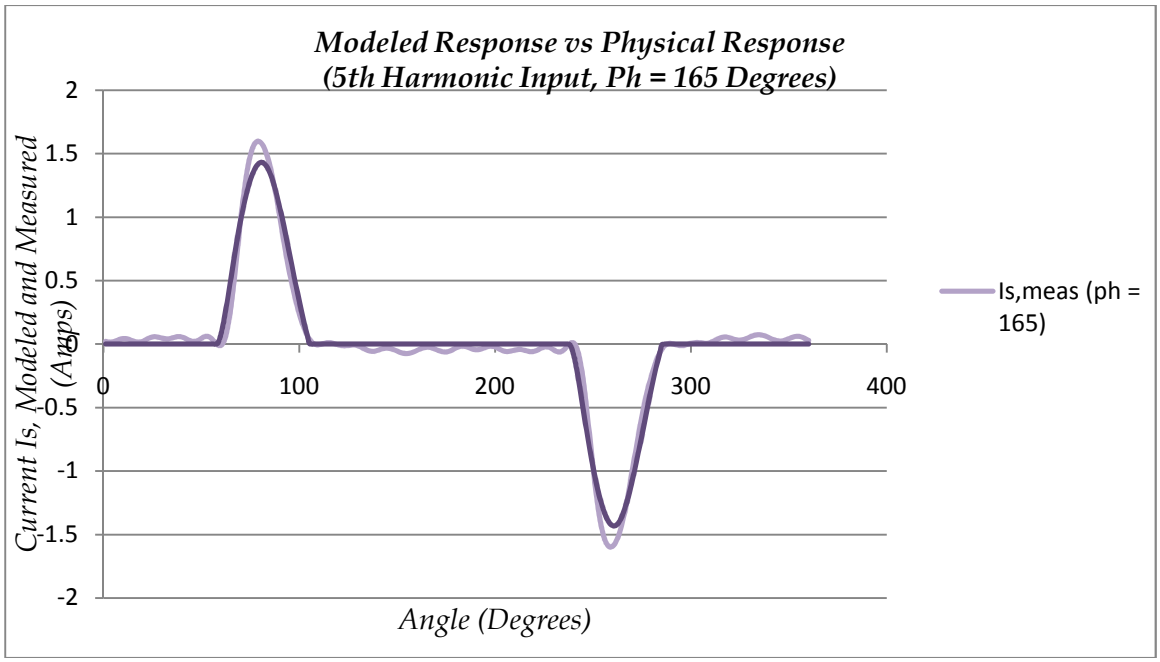



**Figure 6.43: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 5th Harmonic Distortion and Phase Shift = 165°**

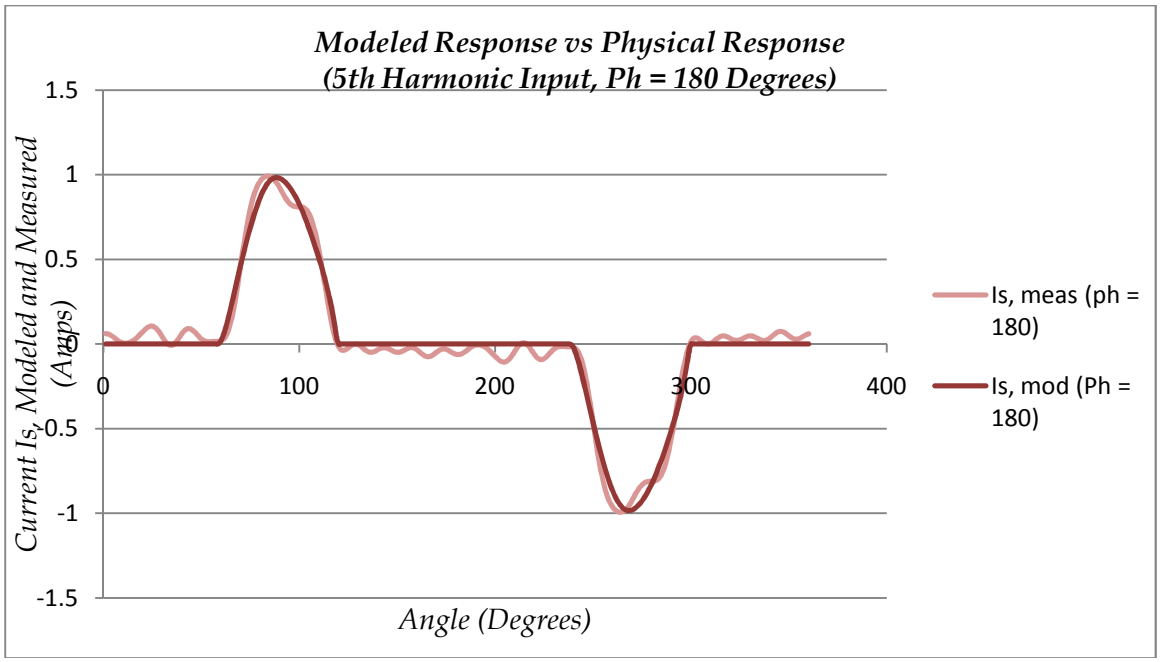



**Figure 6.44: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 5th Harmonic Distortion and Phase Shift = 180°**

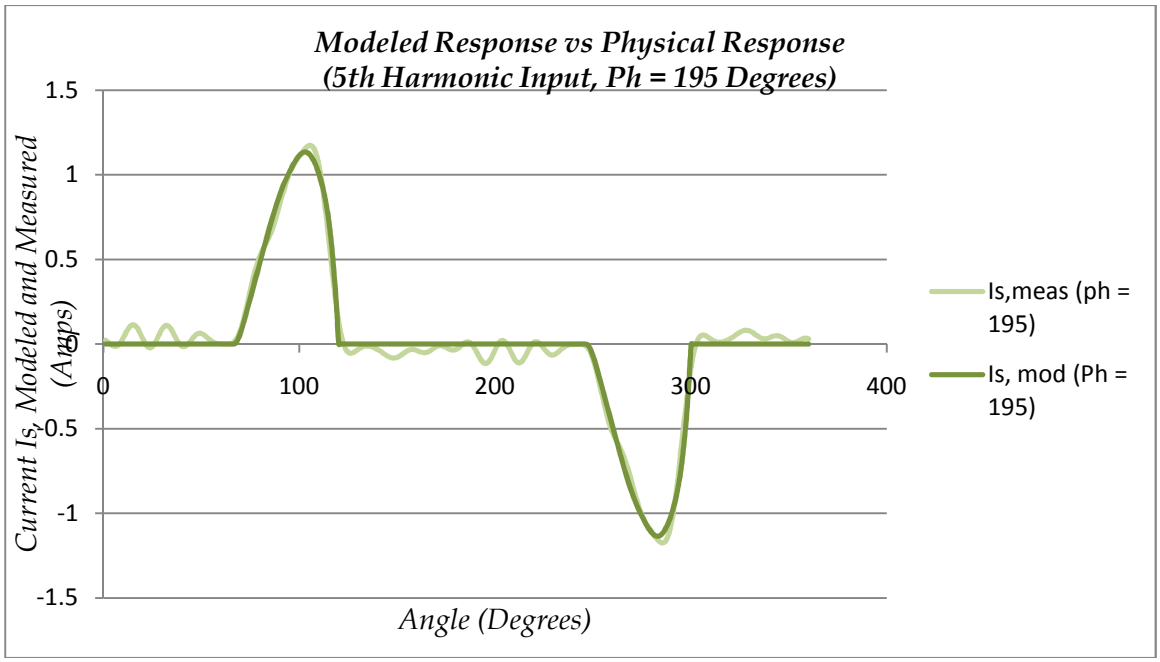



**Figure 6.45: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 5th Harmonic Distortion and Phase Shift = 195°**

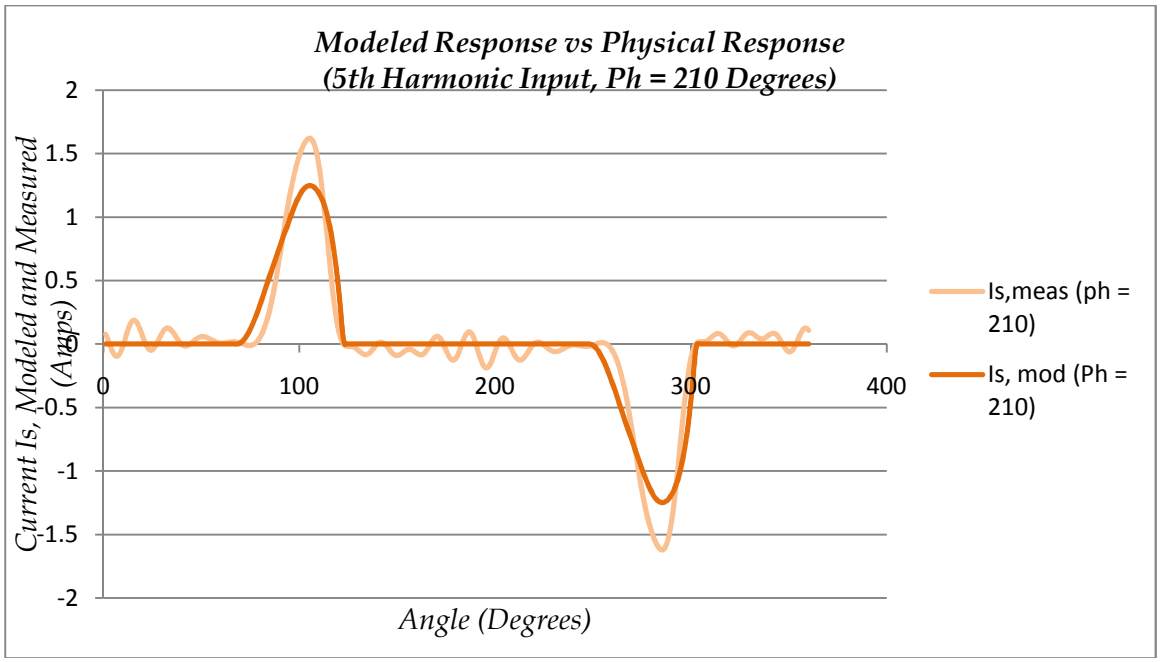



**Figure 6.46: Current Response $I_{S,MOD}$ to a Sinusoidal Supply Voltage with 5th Harmonic Distortion and Phase Shift = 210°**

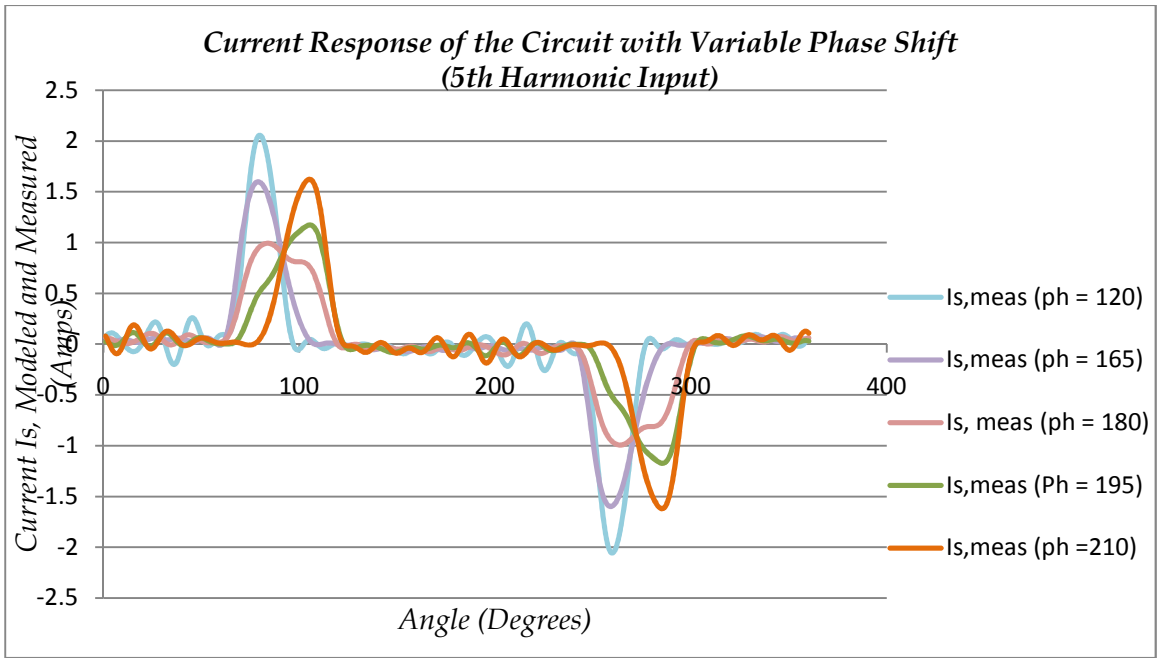



**Figure 6.47: Physical Response $I_{S,MEAS}$ to Varying Phase-Shift = 120°, 165° - 210° for a Sinusoidal Supply Voltage with 5th Harmonic Distortion**

*Conclusion:* The formation of the dual-humped current pulses, at various phase-shifts, can perhaps be attributed to the nature of their input supply voltages. The voltage supply with the 7th harmonic distortion creates a supply voltage curve of two peaks as shown in figures 6.48 and 6.49 respectively. At the instant that the first peak ends, the supply voltage temporarily dips below the capacitance voltage. This signals the discharging capacitor *C* to stop charging, until the second peak of the supply voltage resumes the charging process. The phase-shifts added to the supply voltage influence both the magnitudes of the two peaks of the supply voltages and the instant of their creation, which is why the two humps vary in relation to the variation in the phase-shift. Figures 6.50 and 6.51 illustrate the variation of the harmonic supply voltage with the 5th harmonic distortion added.

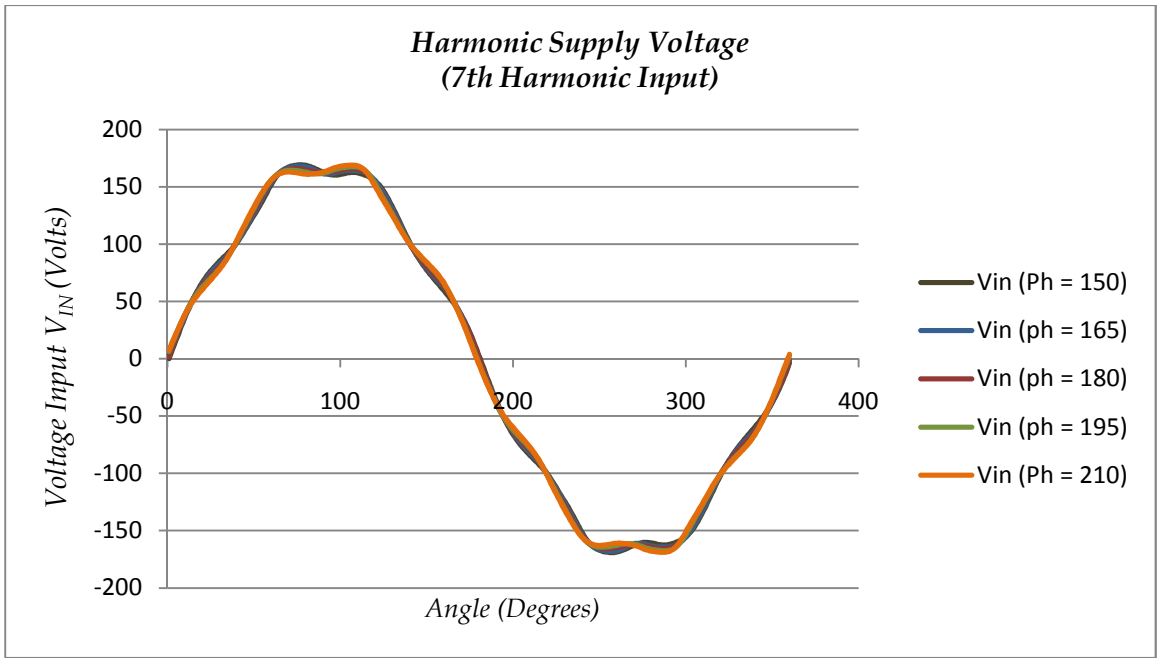



**Figure 6.48: Input Supply Voltage with Varying Phase-Shift = 150° - 210° with 7th Harmonic Distortion**

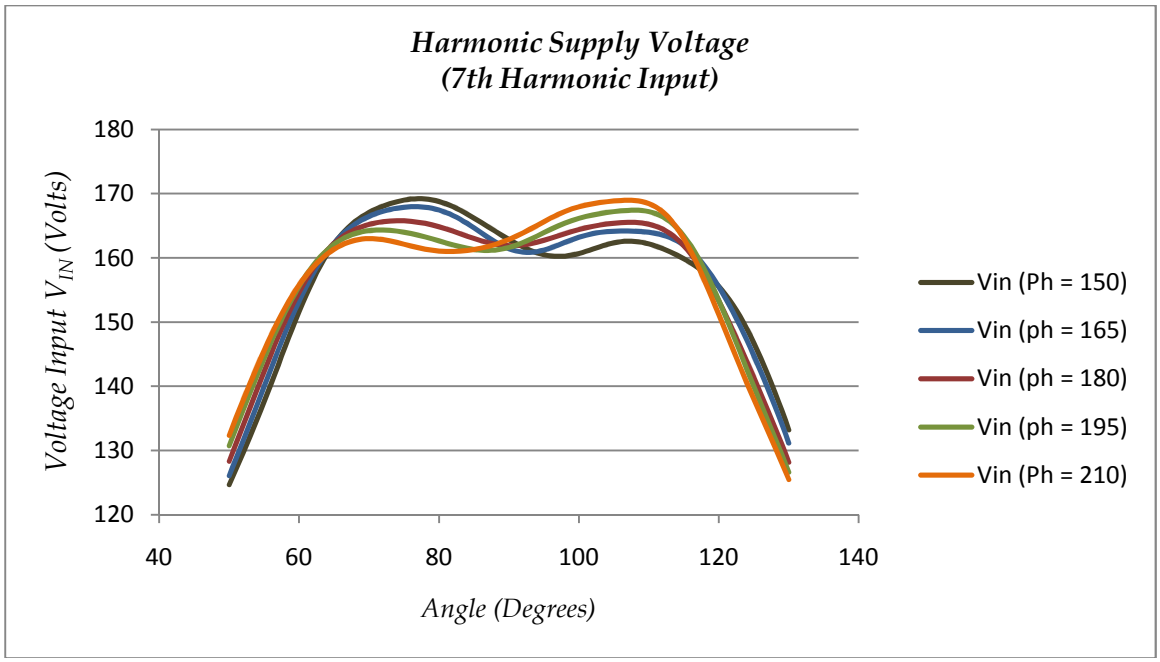



**Figure 6.49: Input Supply Voltage with Varying Phase-Shift = 150° - 210° with 7th Harmonic Distortion (Zoomed-in)**

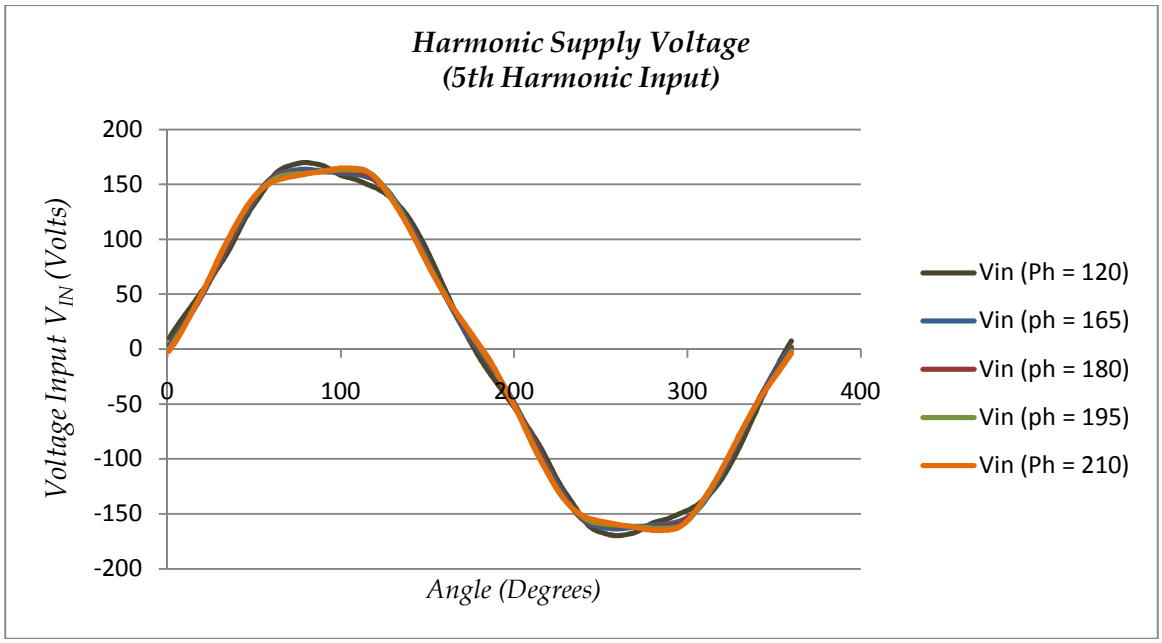



**Figure 6.50: Input Supply Voltage with Varying Phase-Shift = 120°, 165° - 210° with 5th Harmonic Distortion**

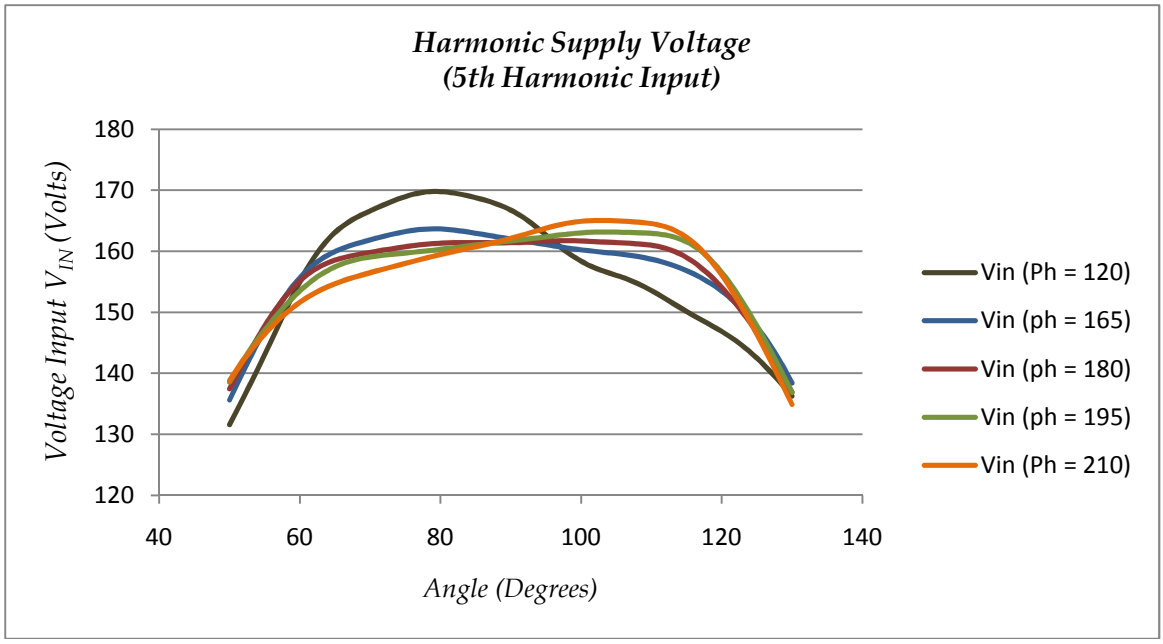



**Figure 6.51: Input Supply Voltage with Varying Phase-Shift = 120°, 165° - 210° with 5th Harmonic Distortion**

## 7. SCENARIO VI: RESPONSE OPTIMIZATION FOR A COMPOSITE POWER ELECTRONICS LOAD CONNECTED TO THE DISTRIBUTION FEEDER NETWORK.

*Scenario Description:* The experimental set-up for this scenario, the theory and the process involved in creating it, are all owing to the research efforts by Dr. M. Rylander and Prof. W. M. Grady.

A composite load – a Fan (60 Hz sinusoidal load) and a Computer Monitor (Power Electronics load) together was subjected to a 25%, laboratory generated, single-phase power electronics load voltage sag. The power electronics load caused distortion in the load response, input current pulse $I_{COMP}$ that momentarily disappears at the onset of the sag. Measured load response, $I_{COMP}$, of the composite load is illustrated in Figure 6.52.

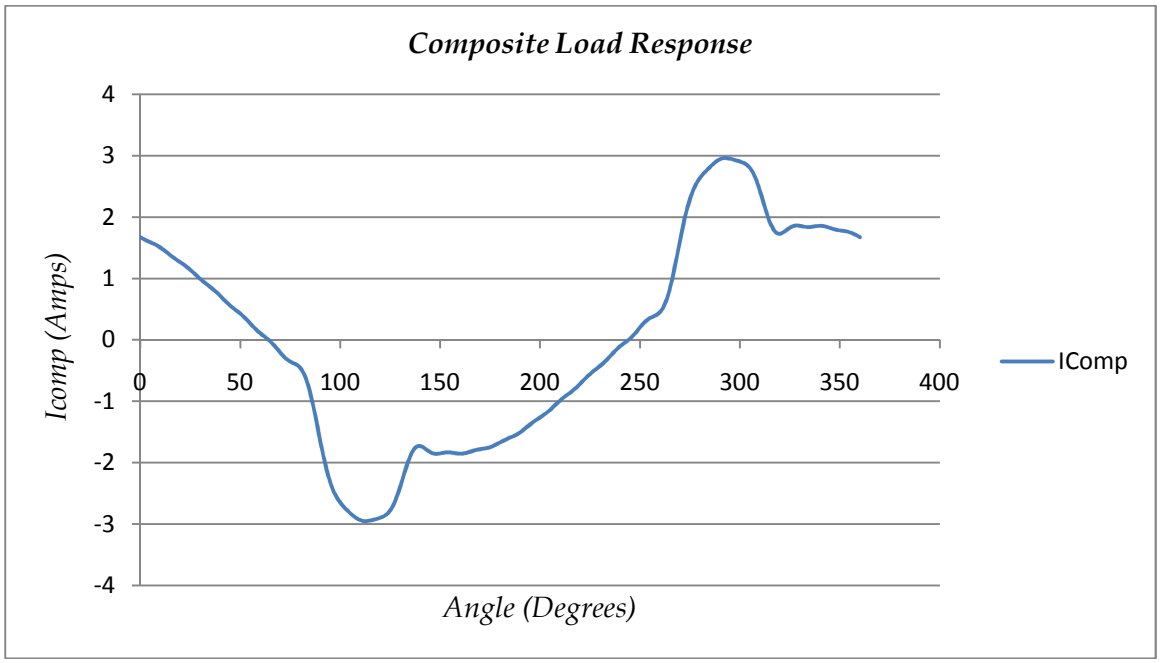



**Figure 6.52: Measured Load Response $I_{COMP}$ of the Composite Load**

This measured load response can be separated into a non-linear component and a linear component, as follows

$$I_{COMP} = I_L + I_{NL} \ldots (4)$$

Where, *L* → *Linear and NL* → *Non-Linear*

We study the pre-sag cycle of the current in order to decompose the composite load response, as illustrated in Figure 6.52. By taking the FFT of this current, we determine the fundamental and the harmonic components of the composite load response, $I_{COMP}$. The two components are illustrated in Figure 6.53 and are also represented by the following equation:

$$I_{COMP} = I_{FUND} + I_{HARM} \ldots (5)$$

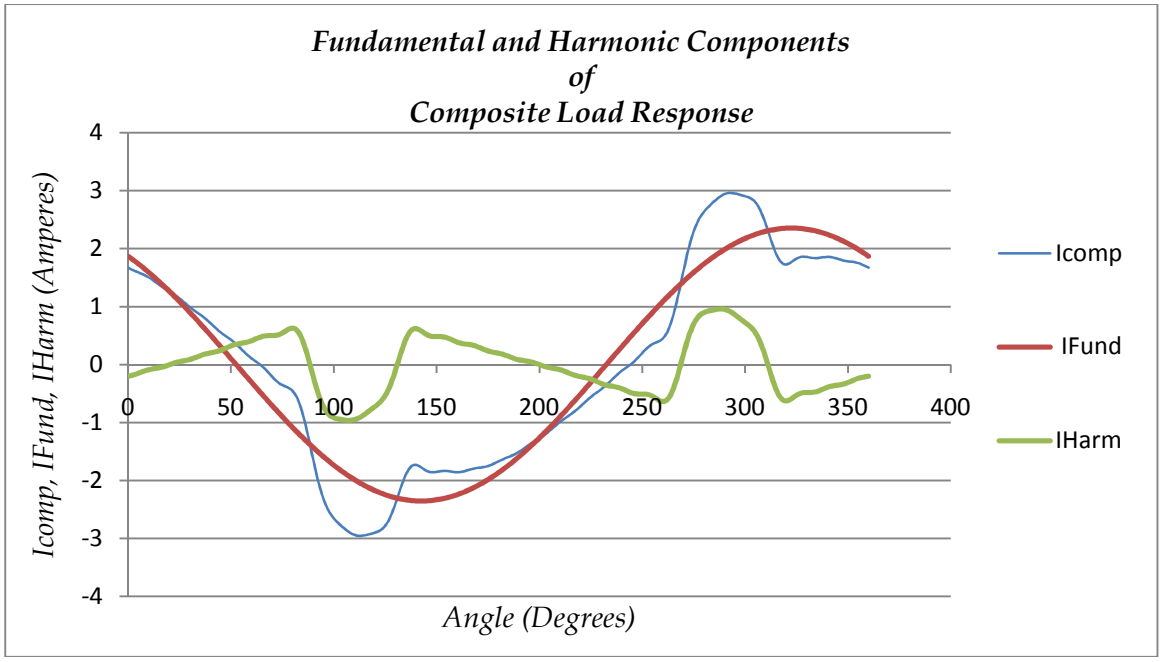



**Figure 6.53: $I_{COMP} = I_{FUND} + I_{HARM}$**

Since the linear component of the composite load is assumed to be an ideal device, it does not contribute to the *Harmonic Component* of the composite input current pulse, the *Harmonic Component* must then be entirely attributable to the non-linear (power-electronics) component of the load. By inference, the harmonic portion of the composite load (as inferred from equation 5) representing the non-linear component of the load, must entail that it be composed only of the harmonics above the fundamental of a non-linear load. Therefore,

$$I_{Harm,NL} = I_{Harm} = \sum_{h=3,5,7\ldots} I_h \ldots (6)$$

The fundamental of the composite load, however, is the sum of fundamentals of the linear and non-linear load. Mathematically, this relationship is expressed as,

$$I_{Fund} = I_{Fund,L} + I_{Fund,NL} \ldots (7)$$

The fundamental component of the non-linear load is determined by calculating the fundamental least-square curve-fit (LSCF) of the discharging-phase (highlighted in figure 6.53) of the *Harmonic Component* curve. The input current pulse during the discharging-phase of the Diode Bridge Rectifier circuit (and therefore the Single-phase power electronics load) is zero. The fundamental component of the input current pulse is, therefore, the inverse of the fundamental curve-fit approximation. Figure 6.54 displays the two curves and

$$I_{Fund,NL} = -Least\ Square\ Curve\ Fit \ldots (8)$$

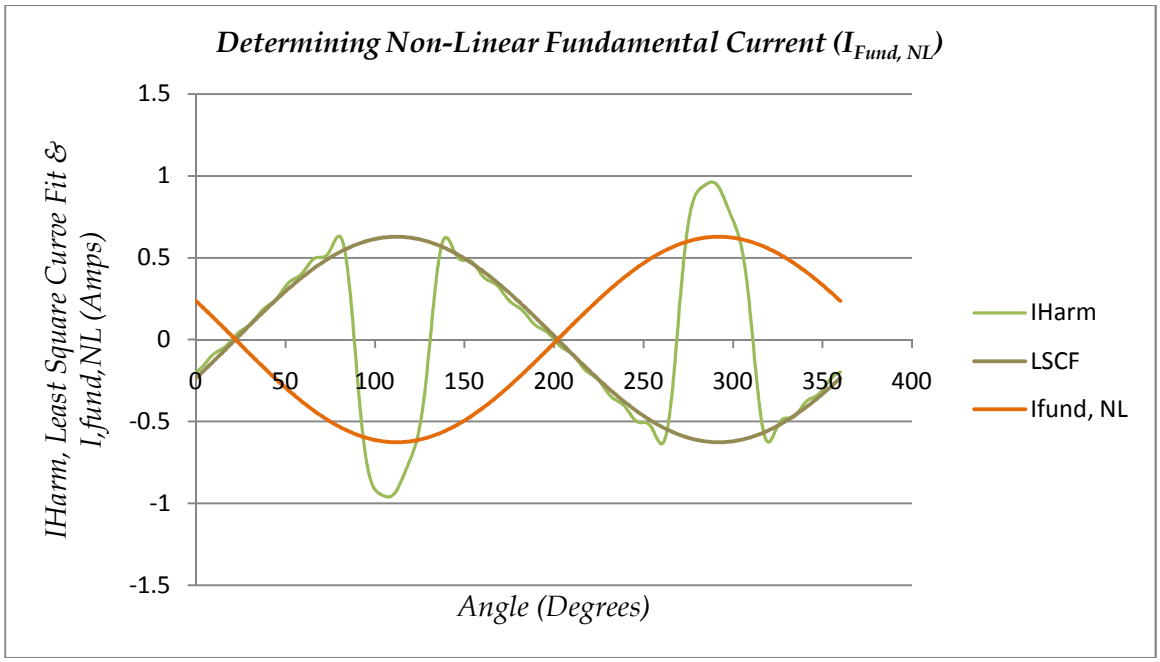



**Figure 6.54: $I_{FUND,NL}$ = -LSCF($I_{HARM}$)**

The fundamental component of the linear load component is thus deduced by calculating the difference between the fundamental of the composite load and fundamental of the non-linear load as derived from equation 7. Figure 6.55 shows the fundamental composite, fundamental linear and fundamental non-linear currents for a 360° cycle.

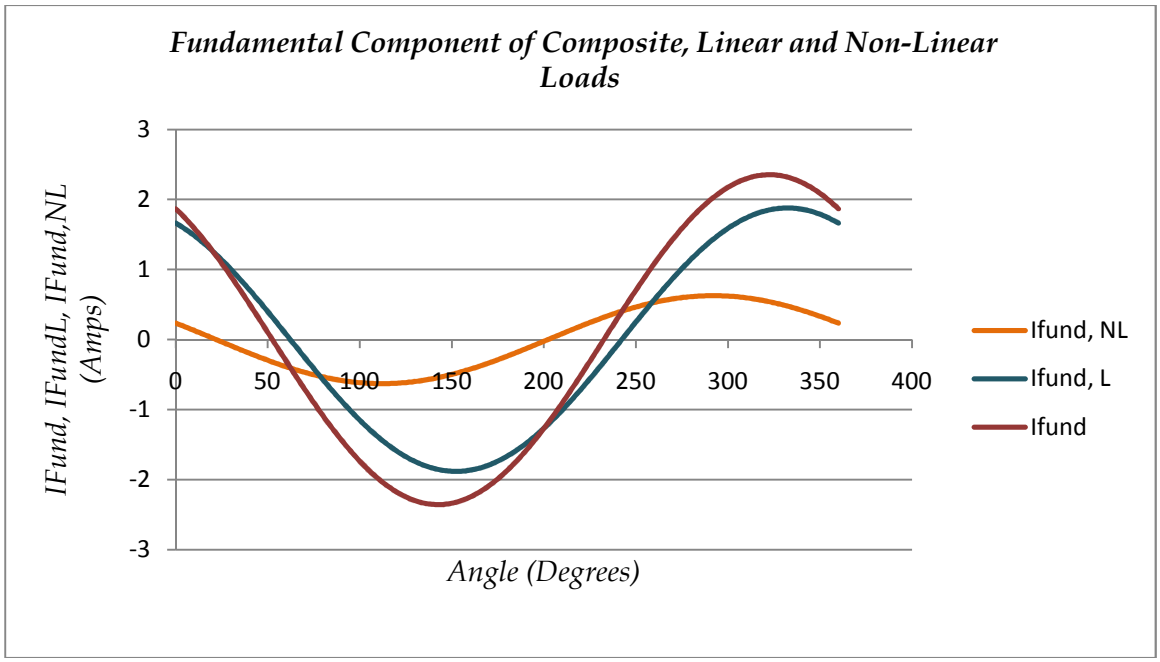



**Figure 6.55:** $I_{Fund} = I_{Fund,\,L} + I_{Fund,\,NL}$

The complete non-linear load response is the sum of the fundamental of the non-linear load and the *Harmonic Component*.

$$I_S = I_{Fund,NL} + I_{Harm,NL} \ldots (9)$$

Figure 6.56 shows the fundamental curve of the linear-load curve and the complete harmonic load response of the non-linear load.

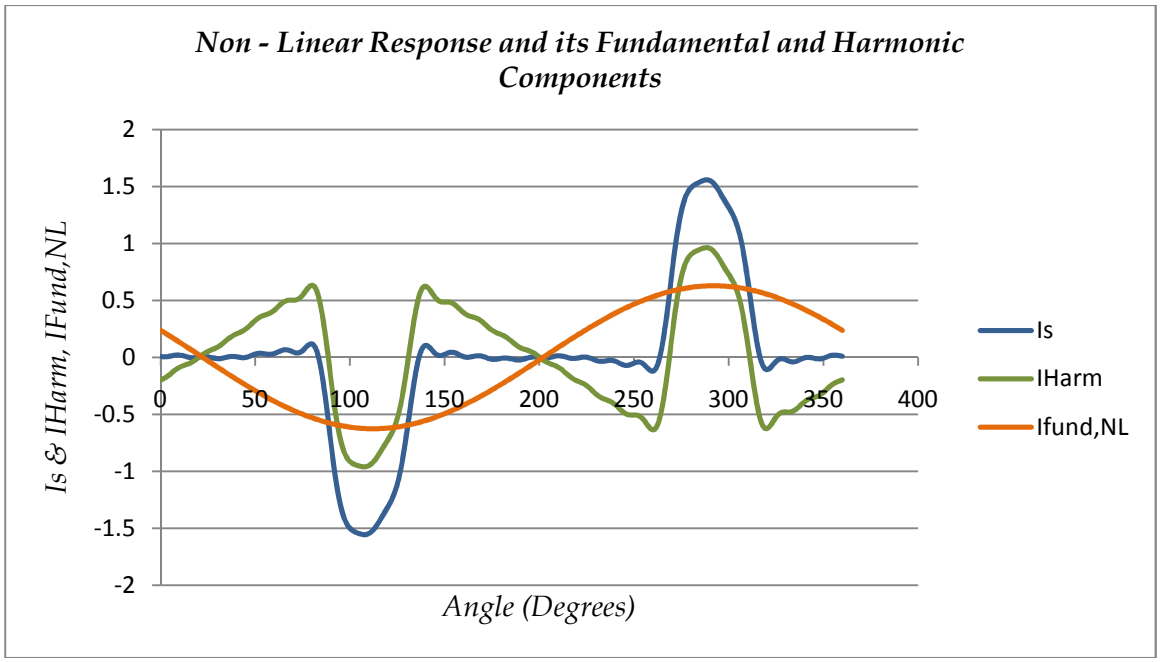



**Figure 6.56: $I_S = I_{FUND,NL} + I_{HARM,NL} = I_{S,MEAS}$**

Once we have segregated the non-linear load response, from the composite load response, we can then use it as as our measured reference current pulse, $I_{S,MEAS}$ to be optimized by automated response algorithms. Figure 6.57 shows us the extent to which the modeled response is optimized to the match the measured load response. Table 6.11 lists the circuit parameters, which are organized by the initial estimate and the collective optimized solution – the *Correction Factor*, for the circuit parameters.

| Parameters | $E_I$ | C | $R_L$ | $R_T$ | $L_T$ |
|---|---|---|---|---|---|
| *Initial Estimate* | 154.96 | 1053.16 | 142.06 | 3.63 | 1.93 |
| *Optimized Solution* | 12.17 | 5012.13 | 478.17 | 1.05 | 12.47 |

**Table 6.11: Optimized Solution of the Circuit Parameters for a Composite Power Electronics Load Added to the Distribution Feeder Network**

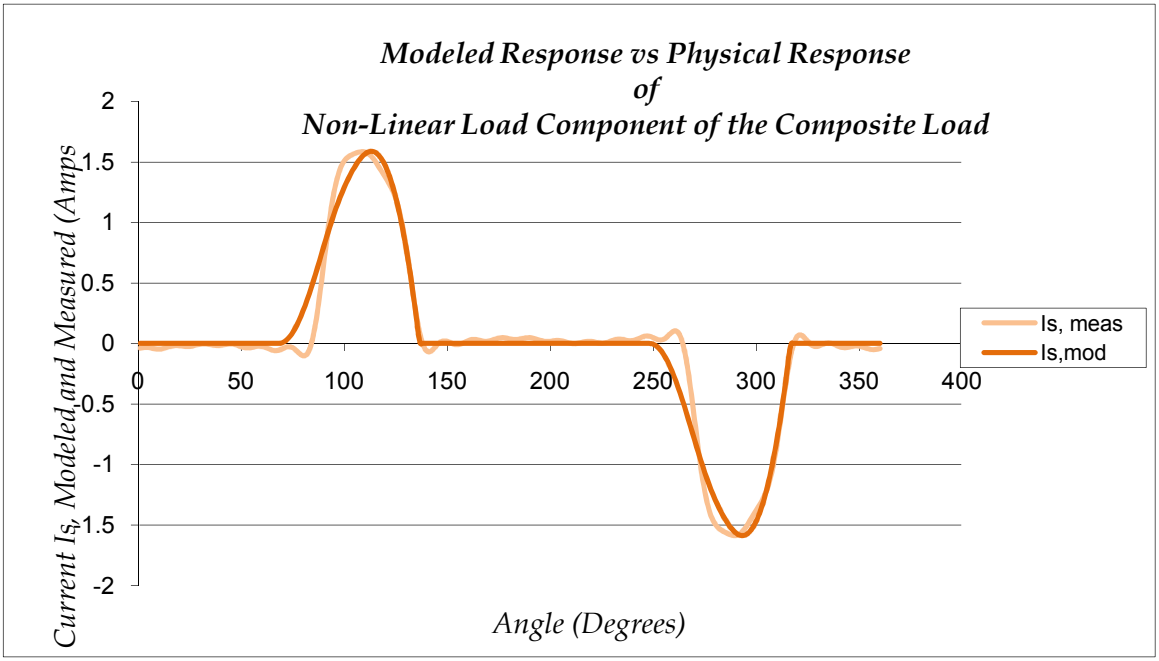



**Figure 6.57: Current Response to the Non-Linear Component of the Composite Load Connected to the Distribution Feeder Network**

## 8. CONCLUSION

The response algorithms, *Load Response, Error Calculation and Response Optimization* that we proposed in Chapter 4, are executed here to create an equivalent circuit model for a multitude of single-phase power electronics loads, powered by a harmonic supply voltage connected at the PCC of a distribution feeder network. We designed five scenarios to evaluate the performance of the *Response Algorithms* in creating a *Correction Factor* that defines the equivalent circuit model. The accuracy of the *Response Algorithms* is measured in terms of the error, $E_I$, which identifies the mismatch between the modeled load response $I_{S,\,MOD}$ and the physical response $I_{S,\,MEAS}$.

Each scenario studies the effect of a constraint variation on the response of the equivalent circuit model, such as the addition of different harmonics to the supply voltage, variation of the load $P_L$, $X/R$ ratio, and the phase-shift in the supply-voltage.

Scenario I demonstrates that the variation of the harmonic content in the supply voltage has an effect on the response of the equivalent circuit model. Little variation was observed in the *Correction Factor* despite the harmonic variation in the supply voltage. The parameters converged to a unique *Correction Factor,* for an equivalent circuit representing a particular set of single-phase power electronics loads connected to the distribution feeder network.

Similar observations were made in Scenarios III and IV respectively.

Scenario III demonstrates the degree of sensitivity of the equivalent circuit to varying load levels. It turns out that load variation has little impact on the response of the equivalent circuit. For the specific set of loads represented by the equivalent circuit model, the parameters consistently converge to a unique *Correction Factor*. Differences in the parameter values between individual load levels are within a narrow range of accuracy.

Scenario IV deals with the effect of *X/R* variation. The parameters converged to a common optimized solution for an *X/R* less than or equal to 1.0. Each parameter variation, however minute, demonstrates a pattern that indicates both the nature of its response and the degree of its sensitivity to *X/R* variation. The Discharging capacitance *C* and the System Inductance, $L_T$, were more sensitive to the X/R variation where-as the Load Resistance $R_L$ and the System Resistance $R_T$ were relatively insensitive to the *X/R* variation. The accuracy in the response of the circuit model was compromised for *X/R* ratios 2 and 5.

The Scenario II effect of the phase-shift variation in the supply voltage on the load response showed that a peakier supply voltage input for a phase-shift = 90°, generates a peakier current pulse with a higher harmonic content than is the case with a flattened

voltage, caused by phase-shift = 180°. The flattened current pulse, in turn, flattens the supply voltage even further, thereby reducing its harmonic content as well. Thus, a cyclical process emerges that could be used to alleviate the harmonic content of the supply voltage and the resultant load response of the equivalent circuit model. This concept is applied to develop the phenomena of *Partial Self- Compensation.*

Scenario V investigated those special cases that are distinguished by the peculiarity of the wave shape of their respective load responses. The most significant of these special responses was a second hump that developed with phase-variation of the supply voltage with the $7^{th}$ harmonic added to it, especially between the 150° - 210° phase shifts. Similarly, peculiarities were also observed with the phase-variation, especially between 120° - 210° in the supply-voltage with the $5^{th}$ harmonic added to it. We can attribute the formation of these peculiar harmonic responses to the typical characteristics of the supply voltages that cause this response. We can only achieve a limited degree of optimization by matching the modeled load response $I_{S,\,MOD}$ with its physical equivalent, $I_{S,MEAS}$ despite the manual correction of multiple parameters simultaneously.

Finally, in Scenario VI, a load combining a linear 60 Hz load and a power electronics load, was connected across the equivalent circuit model after which its load response was analyzed. We can break down the composite input current pulse, $I_{COMP}$ into two components, $I_L$ and $I_{NL}$, corresponding to the contributions of each constituent load. We extracted the non-linear component $I_{S,MEAS} = I_{NL}$ from the composite load response and optimized our initial estimate of the circuit parameters to a *Correction Factor* in order to achieve the matching of a modeled load response $I_{S,MOD}$ to its physical equivalent $I_{S,MEAS}$. Hence, we derived an equivalent circuit for a composite load connected to a distribution feeder network. The data used to create the composite load waveforms for the experiment

was generated using the Harmonics Testing Station. This data is based on the extensive research conducted by Dr. Matthew Rylander and Prof. William M. Grady.

Finally, no significant even harmonics were observed. The presence of any noticeable even harmonic content in the response of a single-phase power electronics load would indicate a system anomaly requiring prompt attention.

# CHAPTER 7

# Conclusion

The proliferation of single-phase power electronics loads has increased the harmonic distortion of the supply current in the distribution feeder network that powers these loads. The interaction of the input sinusoidal voltage with the various collective impedances (the non-linear, impedance of the feeder network, the shared-transformer impedance, the individual branch impedances that connect the loads to the network, and the system impedance of each load) creates harmonic distortion firstly in the supply current and subsequently in each individual branch. Therefore, in order to perform harmonics analysis at a distribution-feeder network, collective harmonic impact of all single-phase power electronics loads connected to the distribution feeder must be considered.

An equivalent circuit model that aggregates all single-phase power electronics loads connected at the point of common coupling is proposed to investigate this problem. This model will simulates all harmonic current-injectors collectively as a single source, and combines their individual contributions as a single composite harmonic signal. This constitutes a *forward* solution that will proactively predict and mitigate the effects of harmonic proliferation into the supply current, which keeps increasing due to the ever larger number of single-phase power electronics loads connected to distribution feeder network.

The equivalent-circuit model represents a distribution-feeder connected to a composite single-phase power electronics load through a diode-bridge rectifier circuit. The rectifier circuit converts input AC voltage to a rectified DC output. This DC output voltage forms the input to the composite power electronics load. The process of AC – DC

rectification of the supply-voltage generates a periodic input current pulse, $I_S$, that charges the smoothing-capacitor of the diode bridge rectifier circuit. This charging current, high in harmonic content, is ultimately injected back into the main current supply, thereby, increasing the harmonic content of the supply.

The input current pulse, $I_S$, determines the response of the equivalent circuit for an input harmonic supply voltage and an optimized solution of the circuit parameters, the latter being collectively labeled as the *Correction Factor*. The accuracy of the model lies in its ability to replicate the aggregate physical input current pulse that powers each individual single-phase power electronics load connected to the network at the point of common coupling.

Our proposed model, thus, will entail the following components: a harmonic voltage source that represents the voltage at the point of common coupling, and the elements of a diode bridge rectifier circuit. The latter consists of a Discharging Capacitance $C$, a system Impedance expressed collectively as $R_{TH} + R_{TRAN}$ and $L_{TH} + L_{TRAN}$, an internal impedance of the rectifier circuit $R_1$ and $L_1$, and the load resistance $R_L$.

The validity of such a model is established by optimizing and matching its simulated response, expressed in terms of $I_S$ (the charging input current pulse) to the actual physical response. A *feed-backwards* method is developed that executes the optimization of the response of the equivalent circuit model. For a particular combination of the circuit parameters also known as the *Correction Factor*, if the simulated response replicates the physical response of the system within a measure of accuracy, the equivalent circuit model is considered valid.

We developed a toolkit of three algorithms, *Load Response*, *Error Calculation* and *Error Optimization,* which we collectively labeled as the *Response Optimization*

*algorithms,* to advance our *feed-backwards* solution. These *Response Optimization algorithms* are at the core of the optimization process. They were designed to manage three phases of the solution: generate the circuit response, $I_S$; compare this response to an actual reference current; and, finally, optimize the circuit parameters to a *Correction Factor* that facilitates a response that matches the reference current. The three algorithms perform the following functions:

- *Load Response* generates the response of the equivalent circuit – input current pulse $I_S$ for both a set of circuit parameters and an input supply voltage. A mathematical expression of the input current pulse is developed as a function of the circuit parameters, $C$, $R_L$, $R_T$ and $L_T$ and the supply voltage $V_{IN}$. This is used to calculate the current pulse $I_S$.

  Our *load Response* algorithm employs a Gauss-Seidel approach to generate the current pulse. It is based upon the operating principles of the diode bridge rectifier circuit.

- *Error Calculation* determines the difference between reference physical response, labeled as $I_{S,MEAS}$ and the modeled circuit response, $I_{S,MOD}$ (determined by the *Load Response* algorithm). This difference is either determined as the sum of differences between the values of two current pulses calculated for each degree in a 360-degrees cycle, or is expressed as the difference between the harmonic (Fourier) coefficients of the two current pulses. The *Error Calculation* algorithm uses the former mechanism as the method of choice

- *Error Optimization* optimizes the circuit parameters $C$, $R_L$, $R_T$ and $L_T$ to a final *Correction Factor* such that the simulated response $I_{S,MOD}$ closely matches the physical response $I_{S,MEAS}$. The *Error Optimization* algorithm minimizes this

difference through an iterative feedback correction mechanism that involves varying the circuit parameters $C$, $R_L$, $R_T$ and $L_T$ sequentially. This algorithm invokes the *Load Response* and *Error Calculation* algorithms during each optimization iteration in order, to determine the corrected response of the equivalent circuit and revise the difference between the simulated response and the reference value.

This process of optimization is analogous to the steepest-descent approach, where in the most sensitive parameter is varied for each iteration to achieve maximum correction. It determines the shortest path that leads to the optimization of the circuit parameters to a *Correction Factor*. An optimized *Correction Factor* generates an accurate simulation of the reference physical model. Once the process of optimization is achieved and verified, the development of the equivalent circuit model is complete.

Accuracy of the *Response Optimization algorithms* is measured in terms of the error, $E_I$, which indicates the difference between the shape of the modeled current replicates the shape of the reference physical current. Five scenarios were designed to evaluate the performance of the *Response Optimization algorithms*. Each scenario illustrates the behavior of the equivalent circuit model under a specific constraint that tests the robustness of the algorithms in creating a valid and accurate circuit model. The following scenarios and their observations are explained below:

- *Scenario I:* Response optimization with varying harmonic content in the supply voltage

The parameters converge to a common solution despite the variation of the supply voltage. Little variation in the *Correction Factor* was observed between

individual cases, each with a different harmonic supply voltage. The parameters converged to a unique *Correction Factor* to model an equivalent circuit that represents a particular set of single-phase power electronics loads connected to the distribution feeder network. Similar observations were made in Scenarios III and IV respectively.

Additionally, the magnitude of the input current pulse increases with each higher harmonic added exclusively to the supply voltage.

- *Scenario II:* Response Optimization with Phase Variation in the Harmonic Supply Voltage

The effect of the phase-shift variation in the supply voltage on the load response showed that a peakier supply voltage input, for a phase-shift = 90°, generates a peakier current pulse with a higher harmonic content than a flattened voltage, caused by phase-shift = 180°. The flattened current pulse, in turn, flattens the supply voltage further thereby reducing its harmonic content as well. Thus, we observe a cyclical process emerge that could be used to alleviate the harmonic content of the supply voltage and the resultant load response, $I_S$, of the equivalent circuit model. This concept is applied to develop the phenomena of *Partial Self- Compensation.*

Harmonic magnitudes of the current pulse for a pure sinusoidal supply voltage were comparable to those of the peaky waveform. However, the peakiness of the current pulse does not affect the shape of the pure sinusoidal voltage waveform, nor does the latter affect the former.

- *Scenario III:* Response optimization with a varying load $P_L$ connected to the equivalent circuit.

Load variation has little impact on the response of the equivalent circuit. For a specific set of loads represented by the equivalent circuit, the parameters consistently converge to a unique *Correction Factor*.

- *Scenario IV:* Response optimization with a varying *X/R* ratio of the equivalent circuit

Little variation in the *Correction Factor* was observed, similar to scenarios I and III. The parameters converged to a common optimized solution for an *X/R* less than or equal to 1.0. Each minute variation in the *Correction Factor*, however, demonstrated a pattern that indicated the nature of its response and its degree of sensitivity to the *X/R* variation. The Discharging capacitance $C$ and the System Inductance $L_T$ were sensitive, whereas the Load Resistance $R_L$ and the System Resistance $R_T$ were constant despite the *X/R* variation. The accuracy in the response of the circuit model, however, was compromised for X/R ratios 2 and 5 respectively. This is indicative of the fact that a realistic solution of parameters exists mostly within an X/R < 1.

- *Scenario V:* Special Cases

Special cases are distinguished by the peculiarity of the wave shape of their respective load responses. In Scenario V these cases were investigated, and it was found that the most significant among these responses was the development of a second hump with the phase-variation of the supply voltage with the $7^{th}$ harmonic added to it, especially between 150° - 210° phase shifts. Similarly, peculiarities were also observed with the phase-variation between, in particular, the 120° - 210°in a supply-voltage with the $5^{th}$ harmonic added to it. The degree of optimization achieved while matching the modeled load response $I_{S,\,MOD}$ with its physical equivalent, $I_{S,MEAS}$

is limited, despite attempts at making manual corrections of multiple parameters simultaneously.

The formation of the dual-humped current pulses, at various phase-shifts, can perhaps be attributed to the nature of their input supply voltages. The voltage supply with the $7^{th}$ harmonic distortion creates a supply voltage curve with two peaks. At the end of the first peak, the supply voltage temporarily dips below the capacitance voltage at that instant. This signals the discharging capacitor $C$ to stop charging, until the appearance of the second peak of the supply voltage resumes the charging process. The phase-shifts added to the supply voltage influence the magnitudes of the two peaks of the supply voltages and instant of their creation; this explains the correspondence of the variation in the two humps to the variation in the phase-shift.

- *Scenario VI:* Response optimization for a composite power electronics load connected to the distribution feeder network.

Finally, in Scenario VI, a load consisting of a combination of a linear 60 Hz load and a power electronics load was connected across the equivalent circuit model, after which its load response was analyzed. The composite input current pulse, $I_{COMP}$ could be theoretically decomposed into the two components, $I_L$ (linear) and $I_{NL}$ (non-linear), which correspond to the contributions of each constituent load. This non-linear component, $I_S = I_{NL}$, was extracted from the composite load response and an initial estimate of the circuit parameters was optimized to a *Correction Factor* such that a modeled load response $I_{S,MOD}$ matched its physical equivalent $I_{S,MEAS}$. The data used to create the composite load waveforms was generated using the Harmonics Testing Station and it is based on the research conducted by Dr. Matthew Rylander and Prof. William M. Grady.

Finally, no significant even harmonics were observed. Presence of any noticeable even harmonic content in the response of a single-phase power electronics load indicates a system anomaly that would require prompt attention.

Once successfully modeled, the equivalent circuit, it is capable of theoretically predicting the current response of N single-phase power electronics loads. For a given voltage supply input at the point of common coupling, the equivalent circuit can emulate these loads. In an alternate scenario, the response of the equivalent circuit model, $I_{L,\,MEAS}$, is optimized to match a reference response designed to restrain the current pulse generated by the equivalent circuit within acceptable harmonic limits. This optimized current signal is subsequently amplified, and it is input to correct the actual load network through the point of common coupling.

A continuous real-time iterative process is thus established, ensuring the optimization of the actual supply current to a desired harmonic content before being injected into the point of common coupling.

Verification and testing of the robustness of the *forward* and the *feed-backwards* solutions was conducted using a *Harmonics Testing Station*. The *Harmonics Testing Station* can be viewed as the experimental equivalent of our proposed analytical model. It simulates the conditions at the PCC with N single-phase power electronics loads connected to it. The model is considered valid if for a given harmonic supply voltage under, an optimized *Correction Factor*, the input current pulse generated by an equivalent circuit model representing a set of multiple single-phase power electronics loads, is consistent with the harmonic response of the same load connected to the *Testing Station*.

The *Harmonics Testing Station* is a LabView based experimental set-up designed to examine the voltage conditions and conduct harmonic mitigation analysis at the point of common coupling (PCC) of a distribution feeder network. It implements a correction mechanism to alleviate the harmonic content of the voltage at PCC, referred to as *Load V*, and match it to a reference voltage signal *Target V,* with a user-defined harmonic content.

The methods of feedback and optimization employed in the *Harmonics Testing Station* share a common objective with the proposed *Response Optimization algorithms* – predicting and optimizing the harmonic current supplied to the distribution feeder network. Hence, they are both applied to evaluate the performance of the *Response Optimization algorithms* and the accurate modeling of the equivalent circuit.

Development of the equivalent circuit model and its *Correction Factor* facilitates the successful compliance testing required by the Harmonics Standards *EN 61000 – 3 – 2*. The harmonic standards require that a pure 60 Hz sine wave voltage signal serve as the voltage supply, which is often difficult to obtain physically. The equivalent circuit model will be able to fulfill that precondition by predicting the harmonic response – the input current pulse $I_S$, for a theoretical 60 Hz sinusoidal input voltage and, thus, ensure a successful albeit theoretical, harmonics testing of a single-phase power electronics load.

# Appendix A

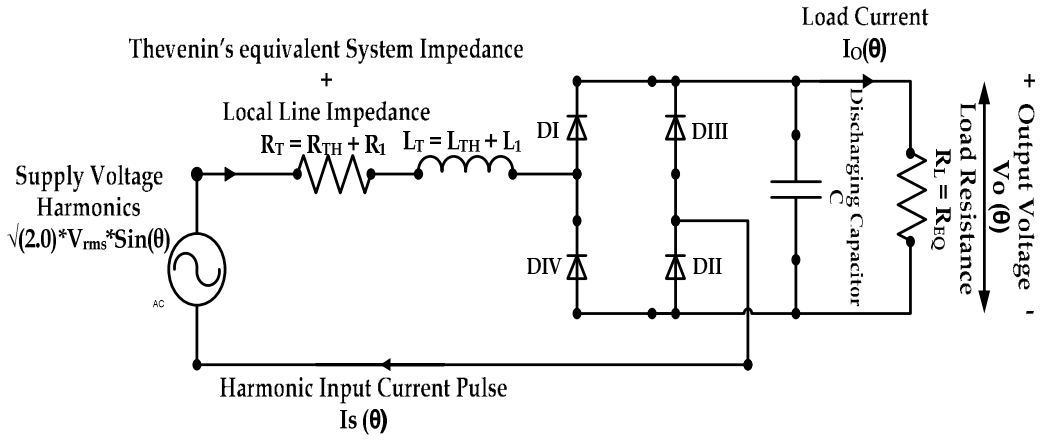



**Figure A1: Capacitor Filtered Diode-Bridge Rectifier Model**

The various circuit components of the given single-phase power electronic load are:

- $V_{TH}$ or $V_S(t)$ – Thevenin equivalent system voltage
- $R_{TH}$, $L_{TH}$ – Thevenin Equivalent system impedance parameters
- $R_1$, $L_1$ – Local Line impedance parameters
- $C$ – Smoothing Capacitor Filtered Diode Bridge Rectifier
- $R_{EQ}$ *or* $R_L$ – Equivalent load resistance

We derive the analytical expressions for the output voltage $V_O(\theta)$ and load current $I_S(\theta)$ $(= I_O)$[11] in terms of the circuit parameters and Thevenin's equivalent of the supply voltage $V_{th}(\theta)$. The circuit is solved for both real and imaginary roots, and the Fourier expression of the input line current is derived analytically.

[11] $I_s(\theta)$ equals $I_o$, as the capacitor current is assumed to be negligible. This assumption is valid as the capacitance $C$ is sufficiently large enough that the charge on the capacitor does not change significantly during the charging and discharging mode.

*Circuit Analysis:* The circuit operates in two modes - *Charging and Discharging*. Input current flows through only during the charging phase, which corresponds to $(\theta_1 \leq \theta \geq \theta_2)$, as shown in Figure A2.

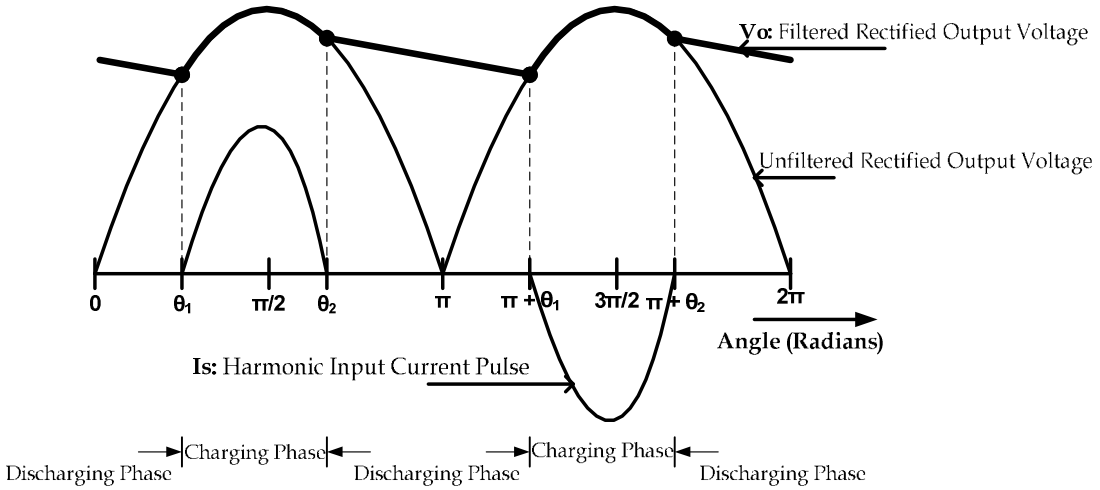



**Figure A2: Charging and Discharging Phases of the Diode Bridge Rectifier Circuit**

*The discharging mode:* $(\theta_2 \rightarrow \pi + \theta_1)$

The capacitor is charged to the peak input voltage at the beginning of the discharging period. Beyond this instant, the input voltage begins to decrease and the capacitor voltage begins to exceed it. The diodes prevent currents from flowing back into the AC side. The capacitor starts discharging through the load connected across it.

At $\theta = \pi$, the input voltage starts increasing again, but its magnitude is still less than that of the capacitor voltage until $\theta = \pi + \theta_1$. At this instant, the capacitor stops discharging, because now the input voltage equals and then exceeds the capacitor voltage magnitude. Thus, the circuit enters the charging mode.

*The charging mode: ($\theta_1 \rightarrow \theta_2$)*

Current $I_S(\theta)$ flows through the diodes and charges the capacitor. The circuit equations are:

$$V_{th}(\theta) = R_t i_s + \omega L_t \frac{d}{d\theta} i_s + V_0(\theta) \quad \ldots \text{(I)}$$

$$is(\theta) = \omega C \frac{d}{d\theta} V_0 + \frac{V_0}{R_{eq}} \quad \ldots \text{(II)}$$

Under non-sinusoidal operating conditions, the supply voltage can be represented as:

$$V_{th}(\theta) = \sqrt{2} \sum_n E(n) \sin\{n\theta + \phi(n)\} \quad \ldots \text{(III)}$$

Where,

$$R_t = R_{th} + R_1, L_t = L_{th} + L_1$$

Equations I and II can be rewritten as:

$$\frac{d}{d\theta} i_s(\theta) = \frac{Vth(\theta)}{\omega L_t} - \frac{R_t}{\omega L_t} i_s(\theta) - \frac{V_0(\theta)}{\omega L_t} \quad \ldots \text{(IV)}$$

and,

$$\frac{d}{d\theta} V_0(\theta) = \frac{i_s(\theta)}{\omega C} - \frac{V_0(\theta)}{\omega C R_{eq}} \quad \ldots \text{(V)}$$

respectively. Equations IV and V can be represented in the Matrix form as:

$$\frac{d}{d\theta}[Y(\theta)] = [\alpha][Y(\theta)] + [\beta][V_{th}(\theta)] \quad \ldots \text{(VI)}$$

where,

$$[Y(\theta)] = \begin{bmatrix} i_s(\theta) \\ V_0(\theta) \end{bmatrix},$$

$$[\alpha] = \begin{bmatrix} -\alpha_1 & -\alpha_2 \\ \alpha_3 & -\alpha_4 \end{bmatrix} = \begin{bmatrix} \frac{-R_t}{\omega L_t} & \frac{-1}{\omega L_t} \\ \frac{1}{\omega C} & \frac{-1}{\omega C R_{eq}} \end{bmatrix},$$

$$[\beta] = \begin{bmatrix} \alpha_2 \\ 0 \end{bmatrix} = \begin{bmatrix} \frac{1}{\omega L_t} \end{bmatrix},$$

$$[V_{th}(\theta)] = \left[ \sqrt{2} \sum_n E(n) \sin\{n\theta + \delta(n)\} \right]$$

*and*

$$\delta(n) = \phi(n) + n\theta_1$$

Laplace transforming equation VI yields:

$$Y(s) = [sI - \alpha]^{-1} Y(\theta_1) + [sI - \alpha]^{-1} \beta V(s)$$

*where*, $\ldots$ (VII)

$$Y(\theta_1) = \begin{bmatrix} i_s(\theta_1) \\ V_0(\theta_1) \end{bmatrix} = \begin{bmatrix} 0 \\ \sqrt{2} \sum_n E(n) \sin\{\delta(n)\} \end{bmatrix}$$

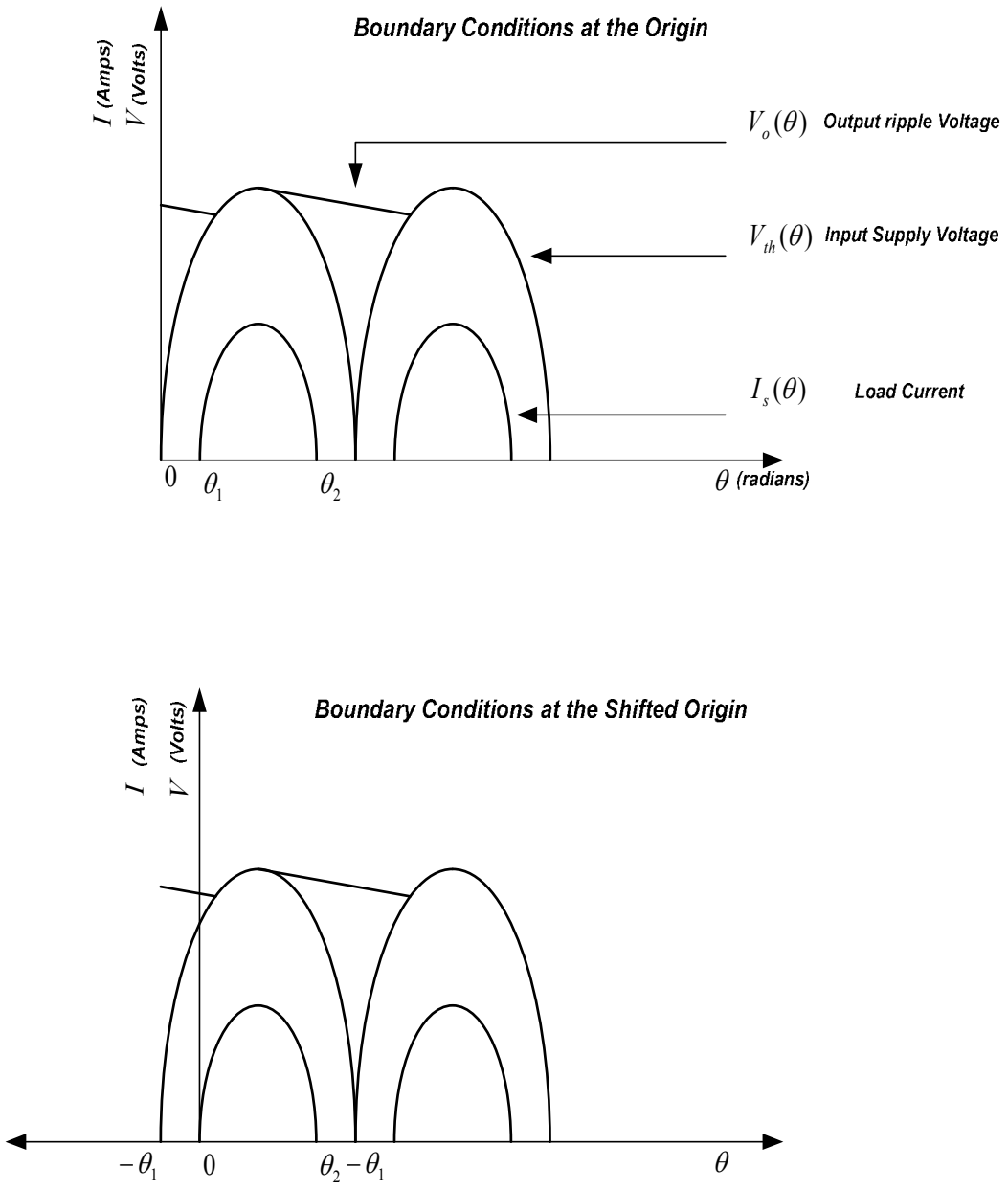



**Figure A3: Boundary Conditions when the origin is shifted to $\theta_1$**

If we shift the origin to $\theta_1$ (refer Figure A3), then the input voltage expression and the initial conditions could be expressed as the following:

$$V_{th}(\theta) = \sqrt{2}\sum_n E(n)\sin(n\theta + \phi(n) + n\theta_1)$$

*and* ... (VIII)

$$Y(0) = \begin{bmatrix} i_s(0) \\ V_0(0) \end{bmatrix} = \begin{bmatrix} 0 \\ \sqrt{2}\sum_n E(n)\sin\{\delta(n)\} \end{bmatrix}$$

The solution for $I_S(t)$ and $V_O(t)$ is obtained by applying the inverse Laplace Transform to equation VIII. Depending upon the values of the circuit parameters, however, the characteristics roots of $[sI - \alpha]^{-1}$ can be real or complex. The characteristic equation for $[sI - \alpha]^{-1}$ can be expressed as:

$$s2 + s(\alpha_1 + \alpha_2) + \alpha_1\alpha_4 + \alpha_2\alpha_3 = 0 \quad \ldots \text{(IX)}$$

The roots of the equation are:

$$s = \frac{-(\alpha_1 + \alpha_4)}{2} \pm \sqrt{\frac{(\alpha_1 - \alpha_4)}{4} - \alpha_2\alpha_3} = a \pm b \quad \ldots \text{(X)}$$

*Case I:* For the roots to be real – $(\alpha_1 - \alpha_4) > 2\sqrt{\alpha_2 \alpha_3}$

Therefore, inverse transforming equation VII yields,

$$i_s(\theta) = \alpha_2\sqrt{2}\sum_n E(n)\left[\begin{array}{l}\left[\frac{e^{(a+b)\theta}}{2b}\left\{-\sin(\delta(n)) + \frac{(a+b+\alpha_4)n\cos(\delta(n))}{a^2+b^2+n^2+2ab} + \frac{(a+b)(a+b+\alpha_4)\sin(\delta(n))}{a^2+b^2+n^2+2ab}\right\}\right] - \\ \left[\frac{e^{(a-b)\theta}}{2b}\left\{-\sin(\delta(n)) + \frac{(a-b+\alpha_4)n\cos(\delta(n))}{a^2+b^2+n^2-2ab} + \frac{(a-b)(a-b+\alpha_4)\sin(\delta(n))}{a^2+b^2+n^2-2ab}\right\}\right] + \\ \cos(n\theta)\left\{\frac{(a^2-b^2-n^2+2a\alpha_4)n\cos(\delta(n)) + (-2an^2+\alpha 4(a^2-b^2-n^2))\sin(\delta(n))}{(a^2+b^2+n^2+2ab)(a^2+b^2+n^2-2ab)}\right\} + \\ \frac{\sin(n\theta)}{n}\left\{\frac{\{(a^2-b^2)\alpha_4 - n^2\alpha_4 - 2an^2\}n\cos(\delta(n)) + \{-2an^2\alpha_4 + n^4 - a^2n^2 + b^2n^2\}\sin(\delta(n))}{(a^2+b^2+n^2+2ab)(a^2+b^2+n^2-2ab)}\right\}\end{array}\right] \quad \ldots \text{(XI)}$$

$$V_0(\theta) = \alpha_2\alpha_3\sqrt{2}\sum_n E(n)\left[\begin{array}{l}\frac{e^{(a+b)\theta}}{2b}\left\{(a+b+\alpha_1)\sin(\delta(n)) + \frac{n\cos(\delta(n))}{a^2+b^2+n^2+2ab} + \frac{(a+b)\sin(\delta(n))}{a^2+b^2+n^2+2ab}\right\} - \\ \frac{e^{(a-b)\theta}}{2b}\left\{(a-b+\alpha_1)\sin(\delta(n)) + \frac{n\cos(\delta(n))}{a^2+b^2+n^2-2ab} + \frac{(a-b)\sin(\delta(n))}{a^2+b^2+n^2-2ab}\right\} + \\ \cos(n\theta)\left\{\frac{(2a)n\cos(\delta(n)) + (a^2-b^2-n^2)\sin(\delta(n))}{(a^2+b^2+n^2+2ab)(a^2+b^2+n^2-2ab)}\right\} + \\ \frac{\sin(n\theta)}{n}\left\{\frac{(a^2-b^2-n^2)n\cos(\delta(n)) - (2an^2)\sin(\delta(n))}{(a^2+b^2+n^2+2ab)(a^2+b^2+n^2-2ab)}\right\}\end{array}\right] \quad \ldots \text{(XII)}$$

*Case II:* For the roots to be imaginary – $(\alpha_1 - \alpha_4) < 2\sqrt{\alpha_2\alpha_3}$

Therefore, inverse transforming equation VII yields,

$$i_s(\theta) = \alpha_2\sqrt{2}\sum_n E(n)\left[\begin{array}{l}\left[\frac{e^{(a+jb)\theta}}{2bj}\left\{-\sin(\delta(n)) + \frac{(a+bj+\alpha_4)n\cos(\delta(n))}{a^2-b^2+n^2+2abj} + \frac{(a+bj)(a+bj+\alpha_4)\sin(\delta(n))}{a^2-b^2+n^2+2abj}\right\}\right] - \\ \left[\frac{e^{(a-jb)\theta}}{2bj}\left\{-\sin(\delta(n)) + \frac{(a-bj+\alpha_4)n\cos(\delta(n))}{a^2-b^2+n^2-2abj} + \frac{(a-bj)(a-bj+\alpha_4)\sin(\delta(n))}{a^2-b^2+n^2-2abj}\right\}\right] + \\ \cos(n\theta)\left\{\frac{(a^2+b^2-n^2+2a\alpha_4)n\cos(\delta(n)) + (-2an^2+\alpha_4(a^2+b^2-n^2))\sin(\delta(n))}{(a^2-b^2+n^2+2abj)(a^2-b^2+n^2-2abj)}\right\} + \\ \frac{\sin(n\theta)}{n}\left\{\frac{\{(a^2+b^2)\alpha_4 - n^2\alpha_4 - 2an^2\}n\cos(\delta(n)) + \{-2an^2\alpha_4 + n^4 - a^2n^2 - b^2n^2\}\sin(\delta(n))}{(a^2-b^2+n^2+2abj)(a^2-b^2+n^2-2abj)}\right\}\end{array}\right]$$

. . . (XIII)

$$V_0(\theta) = \alpha_2\alpha_3\sqrt{2}\sum_n E(n)\left[\begin{array}{l}\frac{e^{(a+jb)\theta}}{2bj}\left\{(a+bj+\alpha_1)\sin(\delta(n)) + \frac{n\cos(\delta(n))}{a^2-b^2+n^2+2abj} + \frac{(a+bj)\sin(\delta(n))}{a^2-b^2+n^2+2abj}\right\} - \\ \frac{e^{(a-jb)\theta}}{2bj}\left\{(a-bj+\alpha_1)\sin(\delta(n)) + \frac{n\cos(\delta(n))}{a^2-b^2+n^2-2abj} + \frac{(a-bj)\sin(\delta(n))}{a^2-b^2+n^2-2abj}\right\} + \\ \cos(n\theta)\left\{\frac{(2a)n\cos(\delta(n)) + (a^2+b^2-n^2)\sin(\delta(n))}{(a^2-b^2+n^2+2abj)(a^2-b^2+n^2-2abj)}\right\} + \\ \frac{\sin(n\theta)}{n}\left\{\frac{(a^2+b^2-n^2)n\cos(\delta(n)) - (2an^2)\sin(\delta(n))}{(a^2-b^2+n^2+2abj)(a^2-b^2+n^2-2abj)}\right\}\end{array}\right]$$

. . . (XIV)

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# Vita

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